

Transformerless series dip/sag compensation with a multilevel cascaded inverter

by

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Thesis presented in partial fulfilment of the requirements for the degree of Master of
Engineering at the University of Stellenbosch.



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December 2001

Declaration

I, the undersigned, hereby declare that the work contained in this thesis is my own original work, unless otherwise stated, and has not previously, in its entirety or in part, been submitted at any university for a degree.

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November 27, 2001

Summary

This thesis covers the development of a multilevel cascaded inverter for the purpose of cost-effective transformerless series dip compensation. Of all known power quality problems, voltage dips are the greatest reason for concern. Dips/sags occur more frequently than outages and therefore tend to be more costly for industry as modern technical equipment becomes all the more sensitive to the quality and reliability of supply. A number of devices already exist to compensate for this problem, but the cost of most of these systems does not always justify the financial losses they compensate for. All of these systems are using transformers and/or large filter components that contribute to the size, price and losses to quite a large extent. Series injection dip compensators offer the advantage of only having to compensate for the decrease in supply voltage during a dip. This results in a significant reduction in the converter ratings and energy storage requirements compared to conventional uninterruptible power supplies or shunt injection power quality devices. Existing inverter topologies, including multilevel inverters, were therefore studied and compared as possible solutions for cost-effective transformerless series dip compensation. On the basis of these considerations the multilevel cascaded inverter seems to be the most cost-effective option. The relatively low harmonic content of its unfiltered output also eliminates the need for a large output filter. A single-phase dip compensator, with this topology, was designed and built according to specifications stated by Eskom, the main utility in South Africa. Batteries as energy storage and automotive MOSFETs as switching components, proved to be most cost-effective options for the specified power ratings. Control algorithms for dip compensation with the multilevel inverter were also developed. Some of these algorithms are based on existing techniques, but two new algorithms were also developed to implement force commutation of the thyristors and to share the power dissipation in the dip compensator. Simulations indicated that these algorithms could be suitable and sufficient for their application. This dip compensator with its control algorithms was tested with a dip generator, developed at the University of Stellenbosch, for different types of loads. The experimental results confirmed the simulations and showed a very good performance for the specified conditions. An optimised design of this dip compensator will make it a cost-effective solution for dip compensation.

Opsomming

Hierdie tesis dek die ontwikkeling van 'n multivlakwisselrigter, in kaskade, met koste-effektiewe transformatorlose duik kompensاسie as mikpunt. Van al die bekende toevoerkwaliteit probleme wek duike in die spanning die meeste kommer. Duike kom meer gereeld voor as kragonderbrekings en neig daarom om 'n groter onkoste te wees vir die industrie soos wat moderne tegnologiese toerusting al hoe meer sensitief raak vir die kwaliteit en betroubaarheid van die toevoer. 'n Aantal toestelle wat vir hierdie probleem kompenseer bestaan reeds, maar die koste van hierdie stelsels regverdig nie altyd die finansiële verliese wat hulle moet elimineer nie. Al hierdie stelsels gebruik transformators en/of groot filter komponente wat grootliks bydra tot die grootte, prys en verliese van hierdie stelsels. Serie-injeksie kompenseerders het die voordeel dat hulle net kompenseer vir die verlies in die toevoerspanning tydens die duik. Dit het 'n beduidende vermindering in die omsetterkenwaardes en energiestoorvereistes tot gevolg in vergelyking met ononderbroke kragbronne (UPS) of nuwe-injeksie toevoerkwaliteit toestelle. Daarom is bestaande wisselrigtertopologië, insluitende multivlakwisselrigters, bestudeer en vergelyk as moontlike oplossings vir koste-effektiewe serie duik-kompensasie. Van al hierdie moontlikhede lyk die multivlakwisselrigter, in kaskade, na die mees koste-effektiewe opsie. Die relatiewe lae harmoniese inhoud van sy ongefilterde uittree elimineer die behoefte aan 'n groot uittreefilter. 'n Enkelfase duik kompenseerder, met hierdie topologie, is ontwerp en gebou volgens die spesifikasies wat vasgestel is deur Eskom, die hoof elektriese kragvoorsiener in Suid-Afrika. Dit het geblyk dat batterye, en MOSFETte uit die motorbedryf, die mees koste-effektiewe opsies bied vir onderskeidelik die energiestoor en skakelkomponente. Beheeralgoritmes vir duik kompensاسie met die multivlakwisselrigter is ook ontwikkel. Sommige van hierdie algoritmes is gebaseer op bestaande tegnieke, maar twee nuwe algoritmes is ook ontwikkel vir die kommutering van die tiristors en die deling van die drywingsverkwisting in die duik kompenseerder. Simulasies dui aan dat hierdie algoritmes geskik en voldoende kan wees vir hulle toepassing. Hierdie duik kompenseerder met sy beheeralgoritmes is getoets vir verskillende tipes laste met 'n duikgenerator wat ontwikkel is by die Universiteit van Stellenbosch. Die eksperimentele resultate bevestig dit wat verkry is uit die simulasies en wys 'n goeie werkverrigting vir die gespesifiseerde kondisies. 'n Geoptimeerde ontwerp van hierdie duik kompenseerder sal dit 'n koste-effektiewe oplossing maak vir duik kompensاسie.

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Acknowledgements

I would like to thank the following people who made this project and thesis a learning as well as a gratifying experience:

Prof. Johan Enslin, Prof. Toit Mouton and Dr Johan Beukes for their guidance;

All my fellow students who made it enjoyable and rewarding to be a part of the PEG group, especially Aniel le Roux and Willie Combrink for their technical advice and Frank Engelbrecht's entertaining phone calls;

Gregor Groenewald for his technical assistance;

Petro Petzer, Jos Weerdenburg and their staff for their effort with the hardware assembly;

William Johannes, who was interrupted numerous times for laboratory equipment;

ESKOM and the FRD for their financial support.

I would also like to thank my family and friends, like Gert and the people in my cell group, Job-aksie, Nelle and Lara for their prayer and moral support.

Above all I would like to thank my Heavenly Father, who promised me a bright future, convinced me to do my Masters degree and made me capable of completing it successfully.

*For I know the thoughts that I think toward you, says the Lord, thoughts of peace and not of evil,
to give you a future and a hope . JER. 29:11*

Glossary

| | |
|---------------------------------|--|
| $^{\circ}\text{C}$ | Degrees Celsius |
| ΔT | temperature rise in the copper |
| $1\Phi, 3\Phi$ | single-phase, three-phase |
| A | Amperè/ Area |
| AC | Alternating Current |
| Ah | Amperè-hour |
| A_{RMS} | Root Mean Square Current |
| ASD | Adjustable Speed Drive |
| C | Capacitance |
| c | heat capacity of the copper |
| $C_{\text{dc}}, C_{\text{BUS}}$ | DC bus capacitance |
| C_{iss} | Gate input capacitance |
| CVT | constant-voltage transformer |
| DC | Direct Current |
| DPF, $\cos\Phi$ | Displacement Power Factor |
| DSP | Digital Signal Processor |
| DVR | Dynamic Voltage Restorer |
| E_{C} | Energy stored in capacitor |
| EMI | Electromagnetic Interference |
| EPLD | Electronic Programmable Logic Device |
| F, mF | Farad, milli-Farad |
| FACTS | Flexible AC Technology Systems |
| FBI | full-bridge inverter |
| FPGA | Field Programmable Gate Array |
| f_{s} | Switching frequency |
| Hz, kHz | Hertz, kilo-Hertz |
| I/O | Input/Output |
| I^2t | Integrated square of the current delivered by the batteries/ dissipated in the MOSFETs |
| $I_{\text{D//}}$ | Total drain current through parallel MOSFETs |
| I_{Fault} | Fault current threshold |
| $I_{\text{LOAD}}, I_{\text{L}}$ | Load current |
| I_{RIPPLE} | Ripple current of capacitors |

| | |
|--------------------------------|---|
| I_{RRC} | Reverse Recovery Current |
| I_S, I_C | Supply, compensation currents |
| I_{THY} | Thyristor current |
| J, kJ, MJ | Joules, kilo-Joules, Mega Joules |
| kV | kilo Volt |
| KVA | kilo Volt-Amperè |
| L | Inductance |
| L_{DIP}, R_{DIP} | Dip generator inductance, resistance |
| L_L | Load inductance |
| m | mass of the copper |
| m^3 | cubic meters |
| M-G | Motor-Generator |
| mH | milli-Henry |
| M_i | Modulation index |
| min | minutes |
| MVA | Mega Volt-Amperè |
| nm | nanometers |
| P | Power |
| Ph-to-ph | Phase-to-phase |
| PLC | Programmable Logic Controller |
| PLL | Phase Locked Loop |
| P_{on} | Conducting losses of MOSFETs |
| P_r | receiving power |
| P_s | sending power/ Switching losses of MOSFETs |
| P_t | Total losses of MOSFETs |
| Q | Energy dissipated in the MOSFETs |
| R | Resistance |
| R_G | Gate resistance |
| R_L | Load resistance |
| RMS/r.m.s. | root mean square |
| R_{on} | On-state resistance of MOSFETs |
| rpm | revolutions per minute |
| $R_{\theta JC}, R_{\theta CS}$ | Junction-to-case, case-to-sink thermal resistance |
| s, ms, μ s, ns | seconds, milli-seconds, micro-seconds, nano-seconds |
| SLGF | Single Line-to-Ground Fault |

| | |
|---------------------------------|--|
| SMES | Superconducting Magnetic Energy Storage |
| SSD | Superconducting Storage Device |
| STATCON | Static Compensator |
| SVC | static var compensator |
| SVG | static var generator |
| t | time |
| T | Time period of periodic waveform |
| THD | Total Harmonic Distortion |
| $t_{c(on)}, t_{c(off)}$ | Turn-on and turn-off times of the MOSFETs |
| t_{on} | Average on-state time duration of MOSFETs |
| t_p | Time period where polarities of the current and voltage differ |
| T_s | Switching period |
| T_{vj} | Virtual junction temperature of thyristor |
| UPFC | Unified Power Flow Conditioner |
| UPS | Uninterruptible Power Supply |
| V, v | Volt, voltage |
| VA | Volt-Ampère |
| V_{ab}, V_{ca}, V_{bc} , etc. | Phase-to-phase voltages |
| V_C | Voltage across capacitor/ Voltage error signal |
| VCO | voltage-controlled oscillator |
| V_{dc}, V_{BUS} | DC bus voltage |
| $V_{DISCHARGE}$ | Voltage loss across ultra capacitor |
| V_{DS} | Drain-source voltage of the MOSFETs |
| V_{GS} | Gate voltage of MOSFETs |
| V_{INJ} | Voltage injected by the multilevel inverter |
| V_L, V_{LOAD} | Load voltage |
| V_{ON} | On-state voltage across MOSFETs |
| V_{OUT}, V_O | Output Voltage |
| V_{pri} | Primary voltage |
| V_r | receiving end voltage |
| v_{REF} | Voltage reference signal |
| V_{RMS} | Root Mean Square Voltage |
| V_S | Supply/ sending end voltage |
| V_{sec} | Secondary voltage |
| V_{SOURCE} | Source Voltage |

| | |
|----------------------------|---------------------------|
| W, kW | Watt, kilo-Watt |
| X_s | Line reactance |
| Z | Impedance |
| Z_L | Load impedance |
| θ_n | Switching angle |
| ρ | mass density, resistivity |
| $\Omega, m\Omega, k\Omega$ | Ohm, milli-ohm, kilo-ohm |

1. Introduction

1.1 Dips* as a power supply reliability problem

The quality of electricity as it is generated is near perfect [D-4]. The generators used have a well-regulated, pure sinusoid output voltage and the frequency is maintained at very tight standards. Modern interconnected networks have adequate redundancy to ensure reliability of the supply, i.e. to make the possibility of blackouts almost negligible. Unfortunately, electricity, as it is transferred to the customer, is subjected to certain phenomena on the power lines that degrade its quality and reliability. Certain loads that are used by customers, like non-linear loads and large motor and heating loads, also contribute to the degradation of the quality and reliability of the supply.

Degraded reliability of the power supply is more severe than degraded quality** [G-1]. The former can be classified into two groups: dips and outages (see Figure 1.1 from [G-1]). Outages have a more severe effect on customer loads, but dips are much more common [D-13]. Voltage dips have been present in the supply ever since the very first power systems, but they have only recently attracted considerable attention [D-18]. They started to become a problem because equipment used in modern industrial plants (process controllers, programmable logic controllers, adjustable speed drives, robotics) had and are still becoming more sensitive to voltage dips as the complexity of the equipment increases [D-14]. Dips cause spurious tripping of these equipment. In particular, computers, process control equipment and adjustable-speed drives are notorious for their sensitivity [D-18]. Even relays and contactors in motors can be sensitive to voltage dips, resulting in shutdown of a process when they drop out [D-14]. Certain industrial plants suffer large financial losses because of these shutdowns. As dips are much more common than outages, it's not hard to realise that the power supply phenomenon with the greatest deleterious impact on customers is that of voltage dips [D-4].

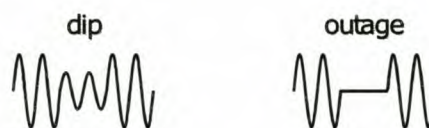


Figure 1.1: *Main power reliability problems.*

* The word 'dip' is most commonly used in South Africa and therefore it will be used throughout this thesis, but it will mean the same as the word 'sag' (commonly used in other countries such as the U.S.A.).

** In general, reliability and quality of the supply are both referred to as power quality.

Voltage dips are already well defined in documents like NRS 048, for the South African utility, and other international documents like IEEE Std 1159. A lot of research work on the causes, occurrence and effects of dips exist ([D-4]-[D-9],[D-11]-[D-17],[D-19]), including research papers on the prediction of voltage dips ([D-1],[D-2],[D-10],[D-18],[D-20]). These research papers mainly show that dips can be minimised but not eliminated and that the occurrence of dips at a site depends on the environment of the nearby power lines. Although there is a rigorous definition and a great deal of knowledge of the problem has been developed, the control of dips within the utility networks is complex, costly and of limited effect [D-4].

Localised compensation solutions at customer sites prove to be more reliable and less expensive [G-1]. These compensation devices can be installed to compensate only for sensitive loads. Among all the existing compensation devices, the group of power electronic converters seems to be the most effective. There are quite a few of these systems available on the market today, but the cost of most of these systems does not always justify the cost of the losses they compensate for. Series power electronic compensators have the advantage of a reduced power rating, and hence reduced cost, to compensate for dips up to a certain specified depth.

From the above it is evident that a cost-effective solution for dip compensation is of the utmost importance and that series compensation devices can be exploited to find such a solution.

1.2 Project background

During the last few years extensive research on power quality compensators, including series compensators, has been done at the University of Stellenbosch [G-1]. All of these systems use transformers and large filter components that contribute to the size, price and losses to quite a large extent. The elimination of the injection transformer and filter components in a series compensator would therefore be ideal in order to reduce its cost.

A new breed of power electronic inverters, called multilevel inverters, provides a solution to this problem. This type of inverter is exploited in this thesis as a cost-effective way of voltage dip compensation.

The objectives of this project are to:

- Determine which multilevel converter topology is the most cost-effective way of transformerless dip compensation;
- Compare available energy storage devices in order to find the most cost-effective device for this application;

- Develop control algorithms for the multilevel inverter for transformerless series dip compensation;
- Develop a protection strategy for transformerless series injection devices;
- Design and built a single-phase laboratory prototype of a 250 kVA transformerless dip compensator in order to verify its performance.

1.3 Thesis outline

This thesis starts by giving a definition of voltage dips in Chapter 2. It also discusses the causes, effects and frequency of dips, followed by an overview of the present solutions for this problem. The latter discussion shows the advantage of series dip compensators: a reduced power rating to compensate for dips up to a specified depth.

Chapter 3 discusses the various possibilities of series dip compensation and explains why the multilevel cascaded inverter is a cost-effective way of transformerless series dip compensation.

The hardware design of the above-mentioned inverter for series dip compensation is explained in Chapter 4. This chapter shows, among other things, why batteries, as energy storage, and automotive MOSFETs, as switching components, are sufficient in terms of cost-effectiveness and performance for the specifications listed at the beginning of this chapter (Chapter 4).

Chapter 5 discusses the control algorithms of the multilevel inverter for series dip compensation. Most of these techniques are based on existing control techniques. Two new techniques are also introduced. Simulations, indicating a very good performance of this system, are also included.

The simulations are confirmed with very good practical results in Chapter 6, showing that this system is fully capable of compensating for dips for various types of loads, according to specifications. Results that confirm the two new control techniques are also included.

2. Voltage dips: Causes, effects and present solutions

2.1 Introduction

In order to compensate for voltage dips, they must be well defined [D-6] in terms of the effects they will have on industries that suffer great losses. Voltage dips may occur on more than one phase simultaneously and may repeat themselves more than once in less than a few seconds, but all of this will cause only one process shutdown event, because of an undervoltage trip of an ASD (adjustable speed drive) or a logic controller. The events that cause voltage dips are also important. Preventative actions can be taken to reduce these events [D-15], but it is impossible to eliminate them [D-4]. If such an event occurs, the dip will be transferred through the network over a certain distance, depending on the voltage level of its origin [D-7]. It will also manifest itself differently at different places on the network, depending on the network configuration and parameters ([D-14],[G-1]). The frequency of these events is another important aspect, because it can give an indication of the financial losses that can be incurred at sensitive industrial plants. The performance and expense of present solutions for voltage dips must then be taken into consideration in order to determine the viability of the solutions. These facts may encourage the quest for new cost-effective solutions.

Paragraph 2.2 starts by categorising voltage dips in terms of certain parameters and also according to national and international standards. It is followed by 2.3, which discusses the causes of voltage dips. This paragraph shows that line electrical faults caused by lightning are the largest single cause for dips on power lines. Paragraph 2.4 follows, explaining the significant effects of voltage dips on certain sensitive equipment in the industry. Information on the frequency of dips, from certain surveys is also given. In 2.5 an overview of the present utility and customer solutions for voltage dips are discussed and compared in order to determine their viability and to provide direction for a search for new cost-effective solutions for dip compensation. The chapter is concluded with a summary.

2.2 Definition of a voltage dip

A voltage dip is defined by its depth, duration and the phase shift that is introduced at the beginning and end of a dip. These parameters are illustrated in Figure 2.1.

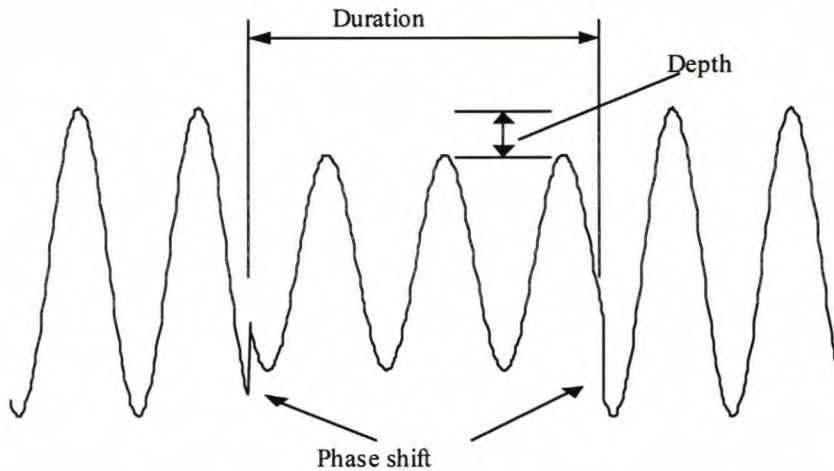


Figure 2.1: *Definition of a voltage dip.*

The depth of a dip can be defined as the percentage value of the maximum difference between the rated r.m.s. voltage and the minimum r.m.s. voltage on all three phases during a dip. This depth can vary [C-17] due to induction motor loads present in industrial systems (see paragraph 2.4). According to IEEE standards [D-6], the depth of a dip ranges from 10% to 90%. If the depth of a dip is more than 90%, it is defined as a momentary interruption.

The duration of a voltage dip is the time measured from the moment the r.m.s. voltage drops below 0.9 pu of declared voltage to when it rises above 0.9 pu of declared voltage. (according to NRS 048 and IEEE specifications). IEEE Std 1159 [D-6] defines the duration of a dip as lasting between a half cycle and 1 min. NRS048 defines it as lasting between 20 ms and 3 s. A voltage loss of a longer duration is defined as insufficient voltage regulation.

There is no specific definition for the phase shift at the beginning and end of the dip, but it can be defined as the worst phase angle between the generated voltage on the utility grid and the voltage waveform during the dip. According to Eskom [D-4], phase shifts of up to 30 degrees have been measured on their system.

The most important parameters of a dip are the depth and duration. The most common way to plot these parameters is on a voltage dip window (see Figure 2.2), when dips are recorded at a site. According to NRS 048: *“For classification purposes, the magnitude of the dip is given by the*

maximum r.m.s. excursion from declared and the duration of the dip is given by the maximum duration of the worst affected phase in each case.” Each recorded dip is represented as a dot.

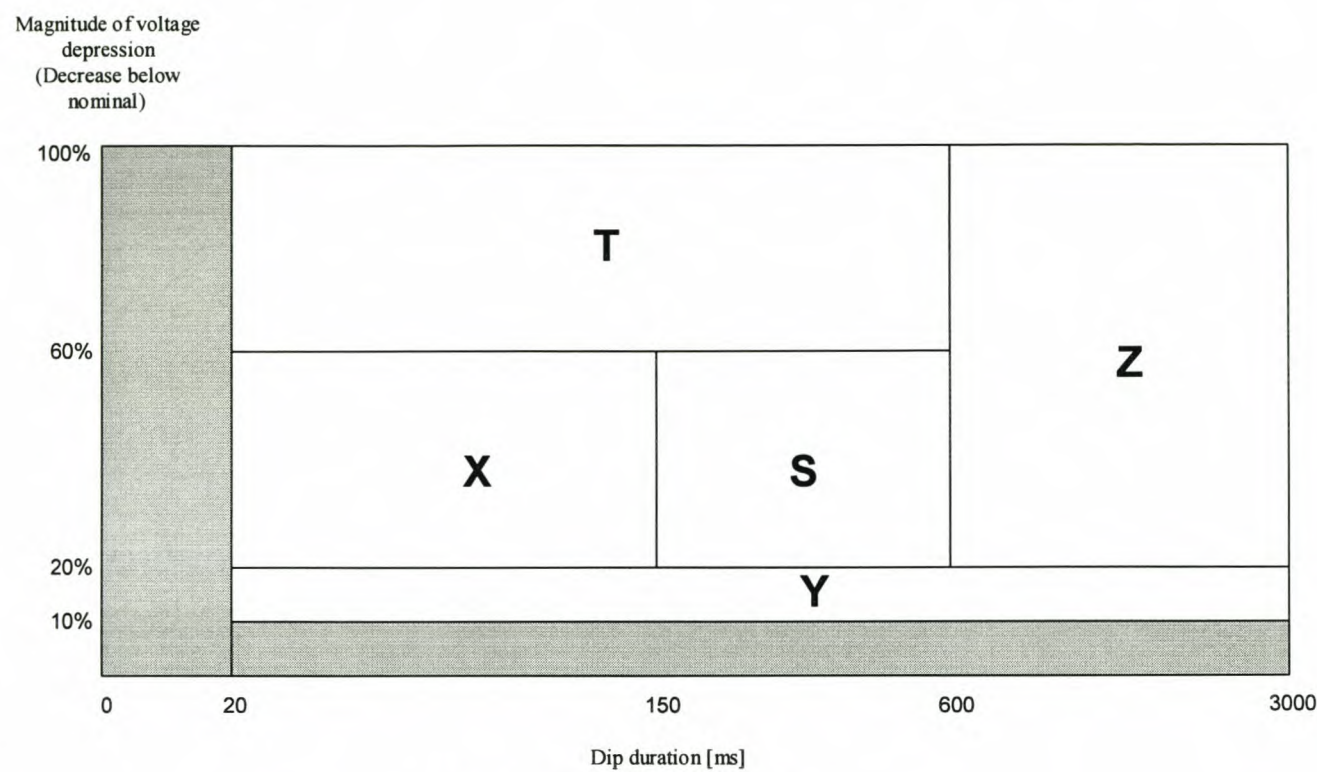


Figure 2.2: Voltage dip window.

The smaller windows (S,T,X,Y,Z) in the voltage dip window are used for purposes of severity classification and contract monitoring [D-4]. This practice was implemented, because early records indicated a clustering of dips in each of the five areas. Specified compatibility levels for each class of dips are given in two extracts from NRS048-2 in Appendix A. Table 2 represents limiting values for each window (S,T,X,Y,Z) for different voltage levels. Table B.1 represents target values for each window for the same ranges. A few typical scatter plots for this voltage dip window are also included in Appendix A.

The parameters that have an influence on the depth, duration and phase shift are discussed, among other things, in the next paragraph.

2.3 Causes of voltage dips

Voltage dips can be categorised by their causes as *supply induced* or *load induced* [G-1].

Supply-induced dips are the most common dips and they are caused by network electrical faults on transmission or distribution lines ([G-1],[D-14],[D-20]). Examples of electrical faults that generate dips are overhead line *flashovers* and *failure of plants* [D-4]. One of the most common causes of *flashovers* is direct or nearby lightning strikes that causes an overvoltage and a resulting breakdown of insulation on overhead line ([D-4],[D-14]). According to [D-15], lightning caused six of the seven dips recorded in one year at an industrial facility in south-eastern Pennsylvania. Other causes of *flashovers* are wind, ice, fires (veld or bush fires and deliberate sugar cane fires), insulator pollution (due to salt mist near coastal areas), mechanical failure, fast-growing vegetation, soil erosion and storm wash-away, animals, sabotage and accidental contact with conductors (through construction or transportation activities).

Plants that fail and cause dips are transformers, circuit breakers, surge arresters and bus bars.

Load-induced dips are caused by a temporary overload of the supply (overload current), like the starting of large motor and/or heating loads by customers [D-4]. This overload current causes a slight voltage drop across the line impedance that can result in a voltage dip [G-1]. An example of large motor loads that cause dips are on-line induction motors that can draw currents of six to ten times their rated value when they are started. The magnetising inrush when large transformers are energised, the cold resistance of large heating loads at start-up and the short-circuiting of electrodes at the start-up of arc furnaces also contribute to the occurrence of load-induced voltage dips.

A power-quality survey on small rural industries [D-12] showed that if a rural site has experienced a high number of voltage dips during the two-week monitoring period, then the majority of the causes are load induced.

A simplified line diagram of a power distribution system is represented in Figure 2.3 [G-1]. This system consists of an infinite bus at the top, which is connected to two parallel feeders (breakers B0-B3) of a transmission network (132 kV). This transmission network is connected to 4 radial feeders (breakers B4-B7) of a distribution network (22 kV) through a transformer. The way an electrical fault introduces a dip can be explained by this figure. A customer that is connected through a transformer to the feeder on the distribution network, which is protected by breaker B4, is considered. This customer will experience a dip during a fault on this feeder (Fault 1), followed by an outage when breaker B4 opens. Most faults are temporary and in such a case the supply will be restored within a few seconds depending on the utility's reclosing practices. If a fault occurs on one of the other feeders (Fault 2, Fault 3), this customer will experience a dip during the time the fault is present and then after the relevant breaker clears the fault, normal voltage will be restored (more

common phenomenon). According to a survey [D-7] remote faults were the cause for 83% of all dips that disrupted solid-state ac and dc adjustable speed drives.

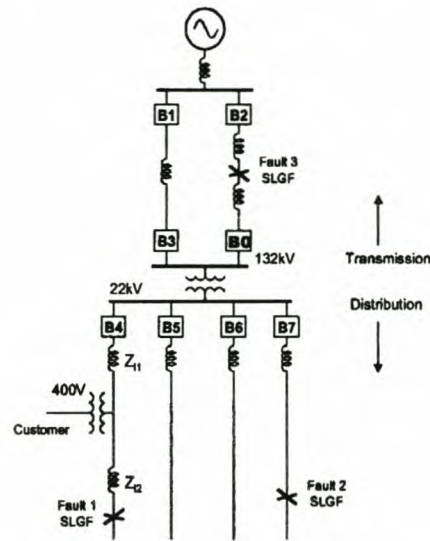


Figure 2.3: Line diagram of simple power distribution system.

Faults on a transmission system, like Fault 3 in Figure 2.3, will affect more customers than faults on a distribution line. However, dips related to faults on transmission lines, compared to those related to faults on distribution lines, are usually more consistent, less disruptive and of a shorter duration, because of looped networks and protection systems with rapid operating times [D-13]. These dips can occur multiple times if reclosing is used by the utility ([D-8],[D-14],[D-20]).

The duration of a dip will depend on its cause, the circuit protection and the nature of the affected plant[D-4]. The inrush currents to remagnetise iron circuits and re-accelerate motor loads can extend the duration of a dip caused by a power system fault.

The depth of the dip and the phase shift depends on the network impedance[G-1] (sum total of the line and transformer reactances involved) and the connections of the transformer[D-14] that is involved, if the fault is far from the transformer closest to the customer. The type of fault (three-phase, line-to-line, SLGF (Single Line-to-Ground Fault) also has an effect on the depth and phase shift ([D-1],[D-14]). Three-phase faults are more severe, but they are less common ([D-13],[D-14]). SLGFs and line-to-line faults are the most common causes of voltage dips.

In reference [D-1] four possible types of dips due to electrical faults are described. Figure 2.4 from [D-1] shows the phasor diagrams for all the types of dips. Table 2.1 [D-1] shows the relationships between fault type, dip type and load connection. The transformation of dips to lower voltage levels through transformers is summarised in Table 2.2. This table shows the type of dip on the secondary

side of each type of transformer for each type of dip. The transformer types are represented with capital letters for the primary connection and small letters for the secondary connection. According to [D-18], in general, the magnitude of the phase jump is indirectly proportional to the distance from the fault and also indirectly proportional to the depth of the dip.

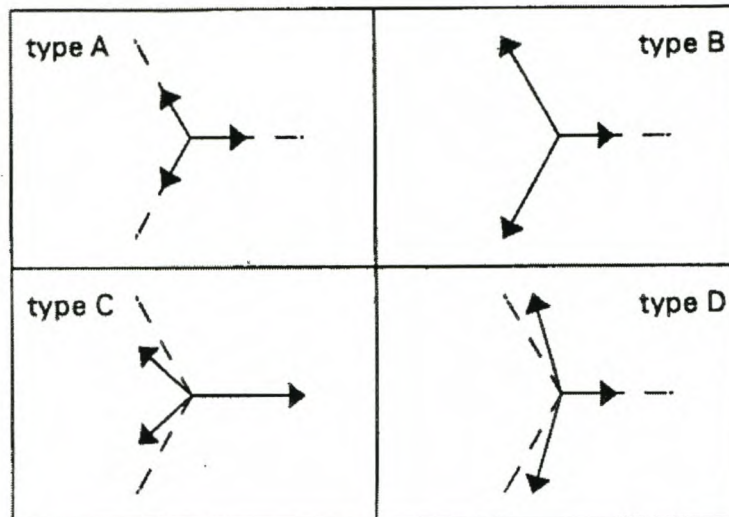


Figure 2.4: Phasor diagrams showing the four types of dips.

Table 2.1: Relationships between the fault type, dip type and load connection for a three-phase load.

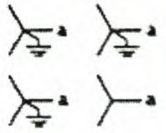
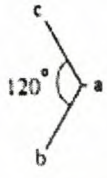
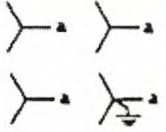
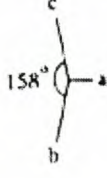
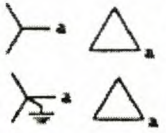

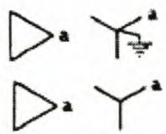
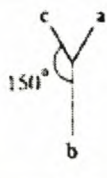
| Fault Type | Load connection | |
|------------|-----------------|-------|
| | star | delta |
| 3-phase | A | A |
| Ph-to-ph | C | D |
| 1-phase | B | C |

Table 2.2: Transformation of dip type to lower voltage levels.

| Transformer Connection | Dip type on primary side | | | |
|------------------------|--------------------------|---|---|---|
| | A | B | C | D |
| YNyn | A | B | C | D |
| Yy,Dd,Dz | A | D | C | D |
| Yd,Dy,Yz | A | C | D | C |

If the fault is close to the primary side of the transformer, closest to the customer, the phase shift and depth of the dip on the secondary side will depend mainly on the transformer connections. Table 2.3 [D-14] represents the most common relationships between a SLGF on the primary of the transformer and the resulting secondary phase voltages. This table can be derived from Table 2.2. It might seem that a SLGF on the primary of a wye-grounded/delta transformer will result in zero voltage across one of the secondary windings. Instead circulating fault currents in the delta secondary windings result in a voltage on each winding.

Table 2.3: *Transformer secondary voltages with an SLGF on the primary.*

| Transformer Connection | Phase to Phase Vab Vbc Vca | | | Phase to Neutral Vab Vbc Vca | | | Phasor Diagram |
|---|-------------------------------|------|------|---------------------------------|------|------|---|
|  | 0.58 | 1.00 | 0.58 | 0.00 | 1.00 | 1.00 |  |
|  | 0.58 | 1.00 | 0.58 | 0.33 | 0.88 | 0.88 |  |
|  | 0.33 | 0.88 | 0.88 | --- | --- | --- |  |
|  | 0.88 | 0.88 | 0.33 | 0.58 | 1.00 | 0.58 |  |

The clustering of dips in the smaller windows of the voltage dip window (Figure 2.2) can be understood in terms of the performance of the protection in a large interconnected network for faults in various locations relative to the dip measurement location. Class X dips are caused by faults remote from the dip location which are rapidly cleared by the protection close to the fault. Such faults are usually large faults, but at the dip location significant parallel infeed maintains a relatively healthy voltage. The lighter dips in the Y-class window are normally load induced and are

most of the time not a reason for concern. Class T dips are caused by large faults local to the dip measurement location, which are cleared rapidly by the protection. Class S dips are usually low-level (e.g. high-resistance) faults cleared slowly by protection such as back-up relays or faults at a lower voltage level, where protection times are longer. Faults in class Z are usually heavy faults or faults at the source end of a radial feed to the dip location that is cleared slowly; Class Z dips usually represent poor or incorrect protection operation.

2.4 Effects and frequency of voltage dips

2.4.1 Effects of dips

It was previously (Chapter 1) stated that disturbances in industries caused by voltage dips are increasing, because of automated control of industrial processes and more complex equipment that becomes increasingly sensitive to voltage dips [D-14]. According to many power-quality surveys, voltage dips become disruptive when the RMS magnitude drops lower than 85-90% of the nominal [D-6]. The sensitivity of these loads also depends on the duration of a dip. Dips from only half a cycle may cause a disturbance [D-14] and even voltage dips with a duration of 4-5 cycles can cause a wide range of sensitive customer equipment to drop out [D-13]. The Computer Business Manufacturers Association in America developed a standard sensitivity curve [D-14], the CBEMA curve (given in Figure 2.5), for disruptive voltage dips. This curve represents the IEEE-446 standard (based on the sensitivity of data-processing computing) for the design of a wide variety of electronic apparatus and computers. It can, however, be expected that different types of equipment and even different brands of an equipment type have different levels of sensitivity.

The voltages experienced during a voltage dip will also depend on the equipment connection (see Figure 2.6 from [D-14]). Table 2.3 showed that the individual phase voltages and phase-to-phase voltages are quite different during an SLGF condition on the transformer primary. Some single-phase loads will therefore be unaffected and other single-phase loads may drop out during a dip, even though their sensitivities to voltage dips may be identical. The sensitivity of a few types of industrial equipment, as described in the literature ([D-1],[D-9],[D-13],[D-14], [D-20]), will be discussed.

a) Motor contactors and electromechanical relays: One manufacturer has provided data that indicate their line of motor contactors will drop out at 50% voltage if the condition lasts for longer

than one cycle. These data should be expected to vary among manufacturers and some contactors can drop out at 70% normal voltage or even higher.

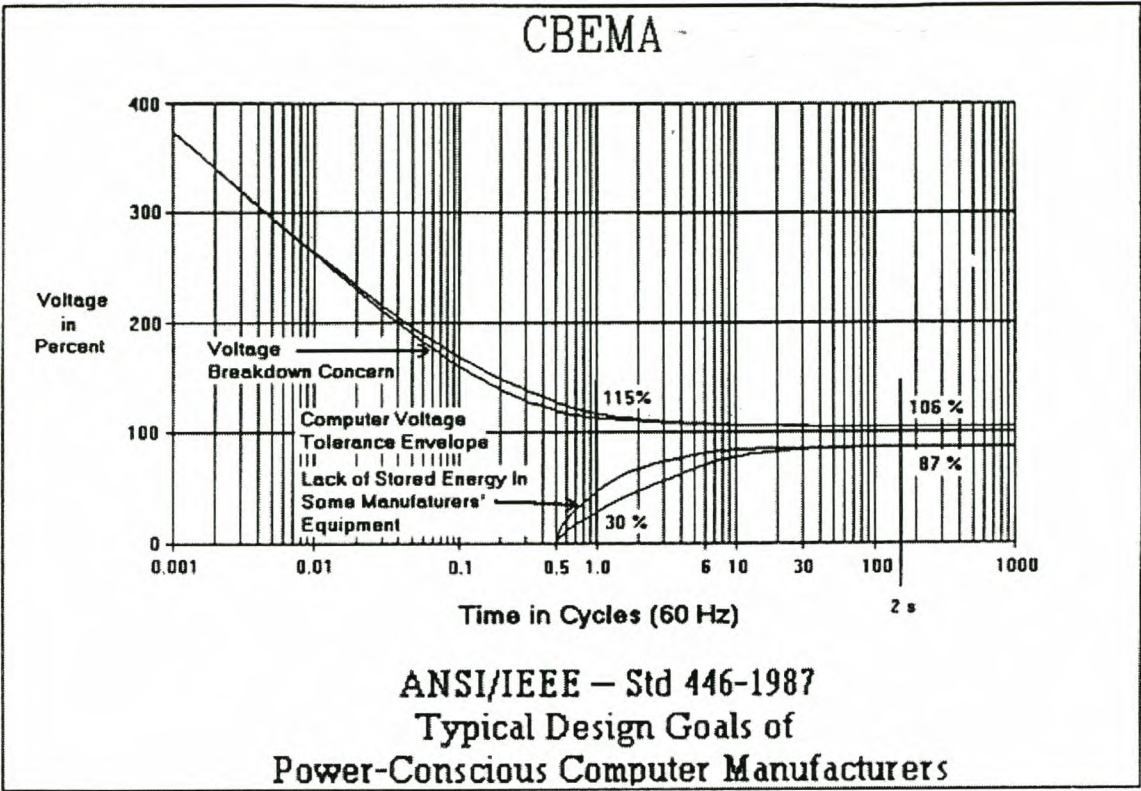


Figure 2.5: CBEMA operating voltage envelope.

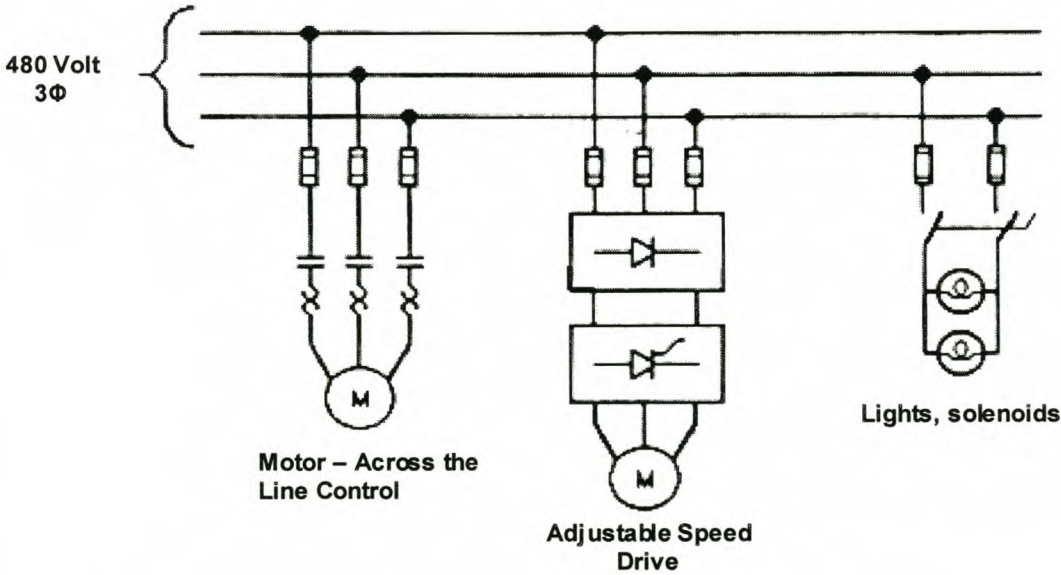


Figure 2.6: Typical single-phase and three-phase loads.

b) Adjustable speed motor drives (ASD's): These drives are used in many industrial processes for a variety of applications. Their sensitivity also differs a lot as illustrated by the results of a survey on manufacturers' data shown in Table 2.4 from [D-7]. Some drives are designed to ride through voltage dips. The ride-through time can be anywhere from 0.05 to 0.5 s, obviously depending on the manufacturer and model. Some models of one manufacturer monitor the ac line and trip after a voltage dip to 90% of the nominal is present for 50 ms.

Table 2.4: *Voltage dip ride-through comparison.*

| Tripout Voltage (% of Nom.) | Outage Survival Time in 60-Hz cycles | Restart into Spinning Motor | Modification to Lengthen Ride-Through Capability |
|--------------------------------|--|--------------------------------------|---|
| None Stated | 1.0 | Optional | Yes |
| None Stated | 3.0 | Yes | Yes |
| Load Dependent | 0.7 | Yes | Yes |
| 70.0 % | 30.0 | Yes | Yes |
| 85.0% | 0.9 | Yes | No |
| None Stated | 9.6 | Yes | Yes |
| None Stated | 0.6 | Yes | Yes |
| 85.0% | 0.5 | Yes | Yes |
| 85.0% | 0.6 | Yes | No |
| None Stated | 0.2 – 1.8 | No | No |
| 75.0% | > 0.5 | Optional | No |
| 85.0% | 3.0 | Optional | No |
| 80.0% | 24.0 | Yes | No |

In one study over a 17-month period [D-9], conducted at two industrial sites with ASDs, it was concluded that voltage dips with a duration of 12 cycles or more and lower than 20% voltage drop will cause an ASD, involved in a continuous process, to trip. These trips can have disastrous effects in many industries, like the plastics extrusion process [D-13], where an interruption can lead to very expensive clean-ups and restarting requirements. Losses can be of the order of \$10 000 per event and a plant fed from a distribution system may experience 20-25 events per year. From preliminary monitoring results it has been determined that certain extruders begin to have problems when the voltage dips to only 88% of the nominal voltage. An example of the sensitivity of these kind of drives is the dip in Figure 2.7 [D-13], which caused a number of dc drives to trip. This figure represents a dip event that is less than a cycle. An ASD doesn't have to trip during a dip to cause damage. In textile and paper mills a brief voltage dip may potentially cause an ASD to introduce speed fluctuations that can damage the end product.

Anecdotal evidence [D-1] indicates that dc drives are more sensitive than ac drives, but this is not documented anywhere. Possible explanations are that dc drives are sensitive to phase-angle jumps as well as drops in voltage magnitude, and that dc drives have less internal energy storage.

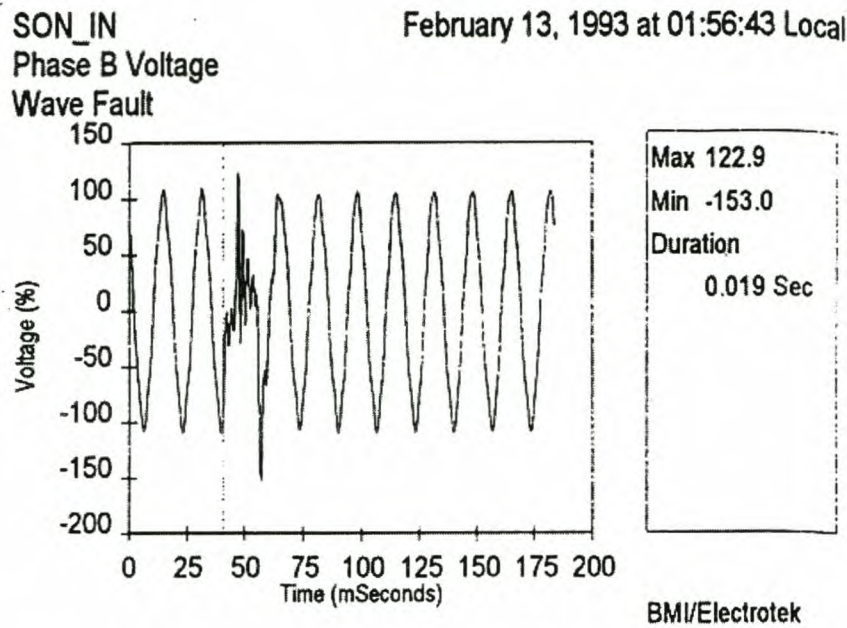


Figure 2.7: Measured voltage dip that caused extruders to trip.

c) *High-intensity discharge (HID) Lamps:* Mercury lamps are extinguished at around 80% of normal voltage and require time to restrike. A voltage dip that extinguishes HID lighting is often mistaken as a longer outage by plant personnel.

d) *Chip testers:* These testers are very sensitive to voltage dips and require 30 minutes or more to restart. In addition, the chips involved in the testing process can be damaged and internal electronic circuit boards in the testers may fail several days later.

An example [D-13] is the 17 voltage dips that caused a loss of load in IBM's sensitive tester room during the 12 months April 1, 1991 through March 31, 1992. The testers were located in a facility fed from a 13.2-kV distribution system. Out of the total of 17 events, 13 were on the 13.2-kV distribution system and 4 were on the 115-kV system. The dips ranged in magnitude from 14-100% below nominal. The testers typically dropped out if the voltage fell below 85% of the nominal.

e) *Process controllers:* These controllers can be very sensitive to voltage dips. A 120 V, 15 VA process controller which regulates water temperature was tested using a voltage dip simulator. The controller was found to be very sensitive to voltage dips, tripping at around 80% voltage, regardless of the duration. The results of this test are shown in Figure 2.8 [D-13].

In one case [D-11], when the voltage levels dipped below 90% of the base value at a particular plant for more than 0.1 s on one or more phases the plant computers were disrupted, resulting in a plant outage.

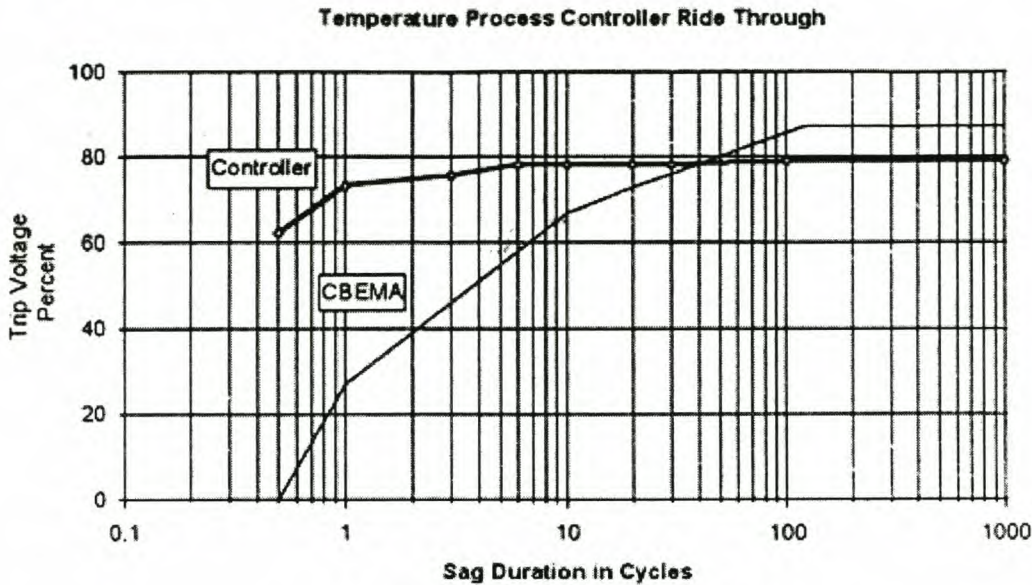


Figure 2.8: Process controller ride-through capability.

f) Programmable logic controllers (PLC's): This is an important category of equipment for industrial processes because the entire process is often under the control of these devices. The sensitivity to voltage dips varies greatly, but portions of an overall PLC system have been found to be very sensitive. The remote I/O units, for instance, have been found to trip for voltages as high as 90% for a few cycles. Figure 2.9 [D-13] shows the results of voltage dip ride-through testing on two different programmable logic controllers. The figure shows the difference between an old and a new version of the same PLC. The newer, type 1 controller is sensitive at 50-60% of nominal voltage, while the older, type 2 PLC could ride through zero voltage for 15 cycles. This illustrates how electronic equipment is becoming more sensitive to voltage variations

g) Machine tools: Machine tools can be very sensitive to voltage variations. A voltage dip can affect the quality of the part that is being machined or it can cause unsafe operation of industrial robots, which need a very constant voltage. These robots' undervoltage protection is often set at 90% of the nominal voltage.

A study of the effects of dips on a whole plant was done in [D-15]. This research and development facility has critical equipment that aids in the process for water fabrication and optical lasers in the 1.3-1.5 nm range. This equipment includes building automation, fire and gas detection systems, temperature controllers and process-related equipment. With highly sensitive power-quality

monitors, the facility recorded seven voltage dips in a one-year period. Lightning caused six of the seven voltage dips, and five of the six dips resulted in equipment failures. Recovery times of 1-3 h were required for voltage dips of less than 300 ms. The effects of the dips were described as follows by the researchers of this study: *"In a critical clean-room process, a power interruption of only a very short duration and magnitude can adversely affect a process. In fact, durations as low as 100 ms with a voltage drop of 25% may only be perceivable as a questionable blink of lights, yet such a voltage sag can initiate a chain reaction of industrial shutdowns and failures that can be catastrophic to a facility's daily profitability."*

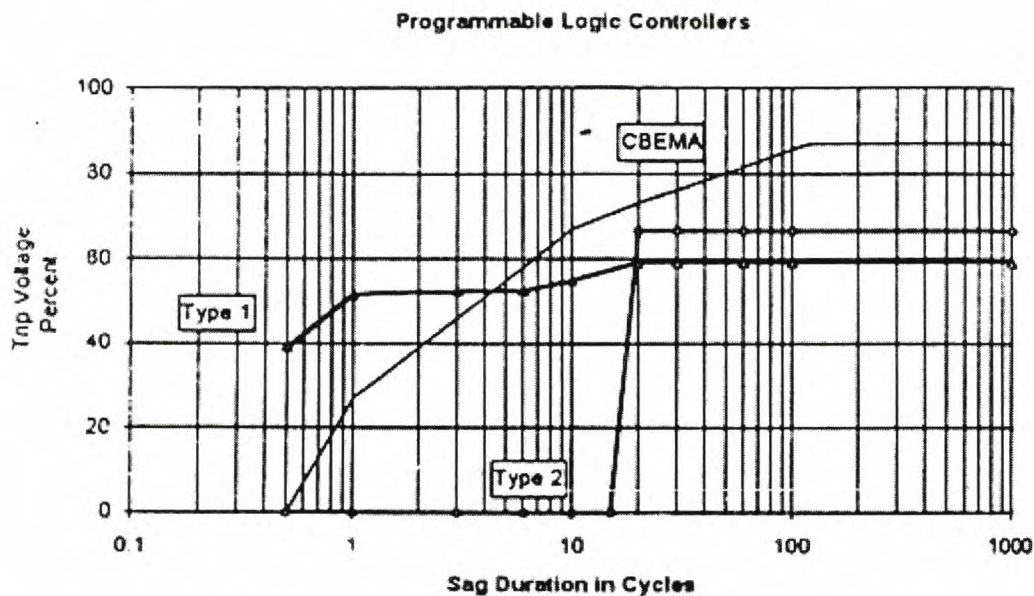


Figure 2.9: Programmable logic controller ride-through capability.

2.4.2 Frequency of dips

In order to get an idea of the production losses caused by voltage dips, the frequency of the dips also has to be taken into consideration.

The frequency of voltage dips at different sites, but also for the same site in different years, can have a wide range because of random factors. It was previously stated that lightning is the biggest cause of voltage dips. The main factors that determine the frequency of voltage dips in a certain area are therefore the intensity of lightning in the area, the length of the lines and the degree of reinforcement on the lines [D-4]. The greater the length of lines in a system, the greater the exposure to dips. This means that system reinforcement, which is usually beneficial from harmonic, fault level and security of supply considerations (availability), can increase the number of dips

experienced. System reinforcement also increases the risk of primary equipment failure due to the increased plant item count.

The total number of dips on the main utility in South Africa for the year 1998 is given in Appendix A. It shows that the northern and central parts of the country, as well as the Eastern Cape, experienced quite a high number of voltage dips, because of a high lightning frequency. The utility in Natal had the most dips, caused by lightning and deliberate sugar cane fires. The Western Cape experienced the least number of dips, which can be attributed to the low lightning frequency.

Three complete case studies from research papers ([D-6],[D-7],[D-11]) on the frequency of voltage dips were studied and are discussed below.

a) EPRI DPQ Project [D-6]

Table 2.5 from [D-6] shows the average number of dips per year per site, worse than or equal to the magnitude and duration headings. These data, supplied by the EPRI DPQ Project, were obtained from monitoring 222 distribution feeders in the United States from June 1, 1993 to June 1, 1994. This table shows that the average site can experience a total of 16.3 dips per year with a voltage magnitude of less than 80% of the nominal and a duration longer than 200 ms. This type of dip will definitely disrupt most of the dip-sensitive equipment discussed before.

Table 2.5: *Sum of dips worse than or equal to magnitude and duration from the EPRI DPQ project.*

| Magnitude | Time in Seconds | | | | |
|-----------|-----------------|------|------|------|------|
| | 0 | 0.2 | 0.4 | 0.6 | 0.8 |
| 90% | 111.2 | 26.7 | 16.8 | 13.2 | 11.7 |
| 80% | 47.8 | 16.3 | 11.2 | 9.6 | 8.8 |
| 70% | 31.0 | 13.7 | 10.4 | 8.9 | 8.4 |
| 60% | 22.9 | 12.4 | 9.9 | 8.6 | 8.2 |
| 50% | 17.9 | 10.9 | 9.4 | 8.3 | 7.9 |
| 40% | 15.7 | 10.0 | 8.9 | 8.0 | 7.6 |
| 30% | 13.6 | 9.5 | 8.5 | 7.7 | 7.3 |
| 20% | 11.4 | 8.5 | 7.7 | 7.1 | 6.9 |
| 10% | 9.8 | 7.9 | 7.2 | 6.6 | 6.4 |

Another interesting fact is that about 88% $((111.2-13.7) / 111.2)$ of the voltage dips (below 90% in magnitude) had a depth of 10-30% (magnitude 70-90%) and a duration of less than 200 ms. Another one-year survey at a single industrial plant [D-13] showed that about 79% of all recorded dips (below 90% in magnitude) had a depth of 10-30%. According to yet another survey [S-7], voltage dips of 10-30% below nominal for 3-30 cycle durations account for the majority of power system disturbances and are the major cause of industry process disruptions. Therefore the probability of

small dips is generally much higher than the probability of large dips because of typical electrical supply configurations [D-7].

b) Canadian National Power Quality Survey [D-11]

A similar type of survey to the EPRI DPQ project was conducted in Canada with a different definition of dips. In the previous surveys a dip on one phase or simultaneous dips on two/three phases of the same feeder were counted as one event. In this survey, however, the number of dips per month per phase per site smaller than 91,6% of the nominal was monitored. Twenty-two utilities across Canada participated in this survey, with a total of 550 sites (industrial, commercial, and residential customer groups) being monitored over a three-year period. The average number of voltage dips per month per phase per site monitored at industrial customers' sites was as follows:

- 38 at secondary voltage levels (i.e. customer side)
- 4 at primary voltage levels (i.e. the utility side).

These figures clearly indicate that most dips are caused by faults on the distribution system. It must also be remembered that a single-phase dip on the primary of a transformer may cause a multi-phase dip on the secondary [D-4]. The former figure (38) is also relative high, because according to [S-5] 68% of all dips are single-phase dips, while 19% are two-phase and 13% are three-phase dips. This will potentially double the type of figures presented in the EPRI DPQ project.

From the commercial site figures in [D-11] more sites at 120/208V had a high frequency of voltage dips than those commercial sites monitored at 347/600V. The average number of voltage dips monitored at commercial utilisation voltages of 120/208 V was higher than those occurring on the primary (e.g. 70% of the sites will experience 2-3 voltage dips on their secondary and only 1-2 voltage dips, on average, on their primary). Voltage dips occurring at 347/600V tended to be equal to those occurring on the primary.

c) Data collection from Indiana transmission lines [D-7]

The findings of another survey that shows the relationship between the voltage levels and the frequency of dips are shown in Table 2.6. This table summarises 16 years of data collected for an average of 5000 miles of transmission lines in Indiana. It shows that the probability of faults on electric lines is indirectly proportional to the voltage level on the line. This is another way to show that the causes of most dips can be related to faults on distribution lines.

Table 2.6: *Relationship between voltage levels and the frequency of dips.*

| Approximate number of transmission line faults per 100 miles per year | | | |
|---|--------|--------|-------|
| 345 kV | 230 kV | 138 kV | 69 kV |
| 3.7 | 2.7 | 4.8 | 9.9 |

In conclusion, the interruption of an industrial process due to a voltage dip can result in very substantial costs to the operation. These costs [D-14] include lost productivity, labour costs for clean-up and restart, damaged product, reduced product quality, delays in delivery and reduced customer satisfaction. According to [S-7], the cumulative cost estimates of power disturbances in the U.S. range from \$20 billion to \$100 billion per year. Industries have reported losses ranging from \$10 000 to \$1 000 000 per disrupting event. An example is one plant [D-7] that had an estimated loss of \$170 600 per year before certain measures were taken. To give an idea of the financial losses in S.A. caused by dips, R.G. Coney of Eskom can be quoted [D-5] as follows : “... in South Africa it is estimated that large industrial customers lose R1.2 billion per annum due to voltage dips ...”

2.5 Existing solutions for voltage dips

According to [D-18], voltage dips should be treated as a compatibility problem between equipment and supply. References [D-13] and [D-6] suggest short-circuit simulations to determine the plant voltage as a function of fault location throughout the power system. Historical fault performance (faults per year per specified distance) can then be used to estimate the number of dips per year that can be expected below a certain magnitude. From these data the effect of dips on equipment in the plant can be determined. Several things can be done by both the utility and customer to reduce the number and severity of voltage dips. Measures can also be taken to reduce the sensitivity of equipment to voltage dips.

2.5.1 Utility Solutions

Utilities can take certain measures to prevent faults that cause dips [D-13]. There are mainly three options to reduce the number and severity of faults on a power system ([D-7], [D-13]).

a) Prevent faults

- Good tree trimming is one way to reduce the number of trees blowing into overhead lines.
- A variety of methods are available to discourage animals from contacting live parts of electrical equipment, like the adding of animal guards.
- Faults due to lightning flashovers can be reduced by lowering the tower or pole footing ground resistance for overhead static wires.
- Insulators on power lines can be washed on a regular basis to prevent contaminated insulators from causing unnecessary flashovers.

b) Modify fault-clearing practices

Improved fault-clearing practices may include adding line reclosers, eliminating fast tripping, adding loop schemes, modifying feeder design and fastening fault clearing through changed time delays for fuses, breakers, etc.

c) Reduce dip magnitudes with delta-wye transformers [D-7]

Three-phase transformer stations that are connected delta-wye or wye-delta alter voltage disturbances.

All of these solutions may reduce the frequency or depth of voltage dips, but will not eliminate them.

2.5.2 Customer solutions

These solutions in the customer's plant can be on a dispersed and integrated basis (distributed solution) or on the basis of a total plant power solution [D-4].

Distributed solution

Essentially a distributed solution involves identifying critical loads and equipment within the customer's plant and integrating targeted energy storage and other solutions at these specific locations / equipment within the plant. An example of this type of solution is to modify ASDs, which are the most common type of dip-sensitive equipment in industrial plants, to make them less sensitive to dips.

Many possibilities exist to improve ASDs' robustness against dips [S-7]. Simple modifications for this purpose are as follows:

- Increased bus capacitance for additional energy during a dip;
- Use of the load inertia to maintain the ASDs' bus voltage at a lower speed during a dip;
- To operate the ASD at a reduced speed/load and thereby extending its ride-through capability;
- Use of lower voltage motors with higher voltage ASDs.

More advanced modifications will be the following :

- An added boost converter on the DC bus with or without energy storage;
- Use of an ASD with an active instead of a passive rectifier on the DC bus to control the DC bus voltage.

Total plant power solution

The total plant power solution involves cleaning up all the power delivered to a facility immediately after the point of supply by the installation of power-conditioning equipment. Power conditioning equipment is used to isolate equipment from high-frequency noise and transient power disturbances, or to provide voltage dip ride-through capability, or both. Proper application of power-conditioning equipment requires an understanding of the capabilities of the device. Also important is a definition of the requirements of sensitive or critical loads. A power conditioner is usually connected only to the feeders with sensitive or critical loads as illustrated in Figure 2.10 [D-13].

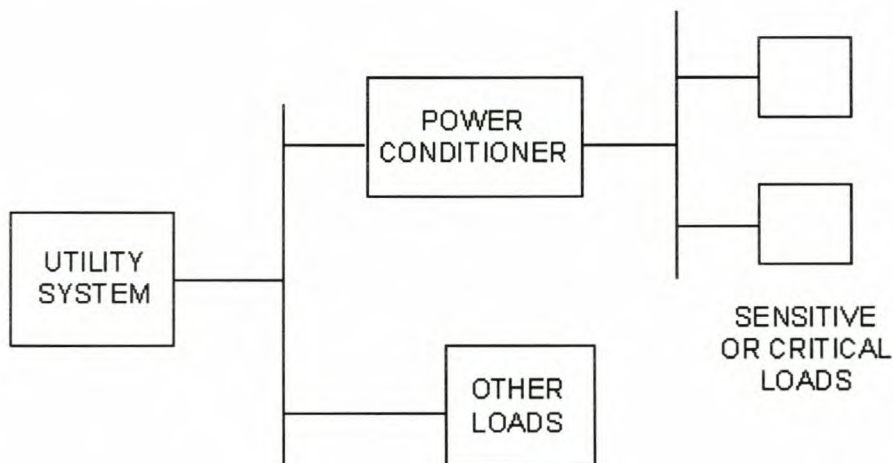


Figure 2.10: *General approach for the application of power-conditioning equipment.*

There are pros and cons to each solution mentioned above which depend on economics, the complexity of the plant, risk, the size of the loads and the managerial/political intent of the utility and the customer. According to [D-4], there are more advantages to a total plant power solution. One power conditioner will be more cost effective and less labour intensive, because in the case of

the distributed solution new equipment will need added attention and expenses. One power conditioner for a total plant power solution at a higher rating than needed will be more viable in most cases.

Many types of power conditioners for voltage dip compensation exist and will now be discussed. A new range of power conditioners, called active filters, is also part of this discussion (*g-i*). Most of these technologies are industrialised and commercially available. In some of the cases, examples of these types of equipment are provided.

a) Tap changing transformers [S-4]

This is one of the most common types of voltage regulators used in today's power distribution systems. The basic configuration of these transformers is illustrated in Figure 2.11. The secondary winding have a few taps, which are all connected to the load via anti-parallel thyristors. Only one of these pairs of thyristors is controlled to conduct, depending on the voltage on the primary side. However, this method has significant shortcomings. For instance, the tap-changing transformer requires a large number of thyristors, which results in highly complex operation for fast response. Furthermore, it has very poor transient voltage rejection and its response to dips is too slow. It is therefore more sufficient for voltage regulation.

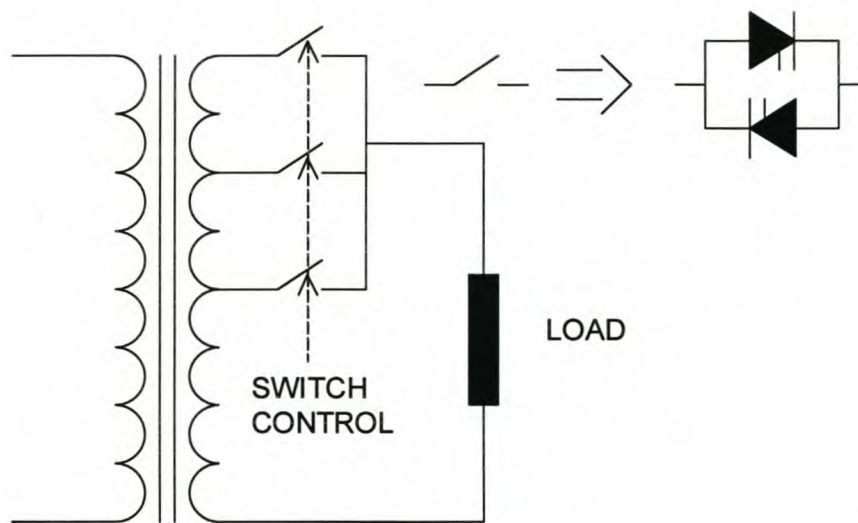


Figure 2.11: Basic configuration of a tap-changing transformer.

b) Ferroresonant transformers (CVTs) ([D-3],[D-8])

Ferroresonant transformers, also called constant-voltage transformers (CVTs), can handle certain voltage dip conditions. They are basically 1:1 transformers that are excited high on their saturation curves, thereby providing an output voltage that is not significantly affected by input voltage

variations. Figure 2.12a [D-3] shows the basic configuration of a ferroresonant transformer. This transformer has a third winding with a large capacitor. The effect of this capacitor is explained in Figure 2.12b [D-3]. This figure shows the characteristic curve of the nonlinear inductance of the third winding together with that of the capacitor at a certain frequency (power system frequency in this case). The operating point where the two curves intersect is independent of the supply voltage, thus the flux through the iron core is independent of the supply voltage (assuming that the ferroresonant winding has a smaller leakage than the input winding). The output voltage is related to this flux, thus also independent of the input voltage.

The energy stored in the ferroresonant winding is able to provide some ride-through during voltage dips. A disadvantage of a ferroresonant transformer is its dependence on load changes. The inrush current of the load can lead to a collapse of flux and a long undervoltage. A modern version of the ferroresonant transformer uses power electronic converters to keep the load current at unity power factor, thus optimising the operation of the transformer.

Ferroresonant transformers should also be sized about four times greater than the load, because the amount of possible compensation (depth of the dip) is indirectly proportional to the size of the load.

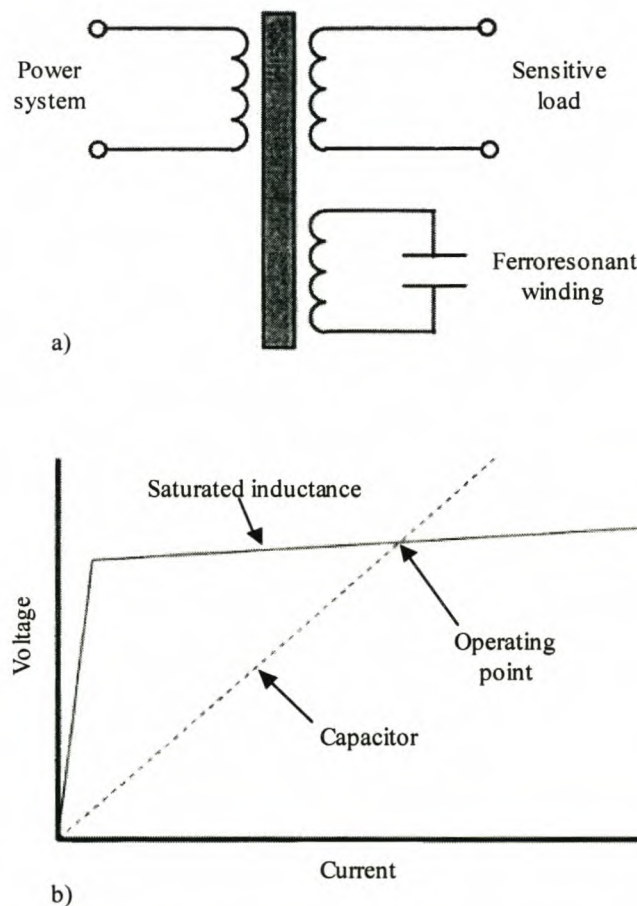


Figure 2.12: *Ferroresonant constant-voltage transformer.*

c) Magnetic synthesisers [D-8]

The magnetic synthesiser is an electromagnetic device which takes incoming power and regenerates a clean, three-phase ac output waveform, regardless of input power quality. A block diagram of the process is shown in Figure 2.13.

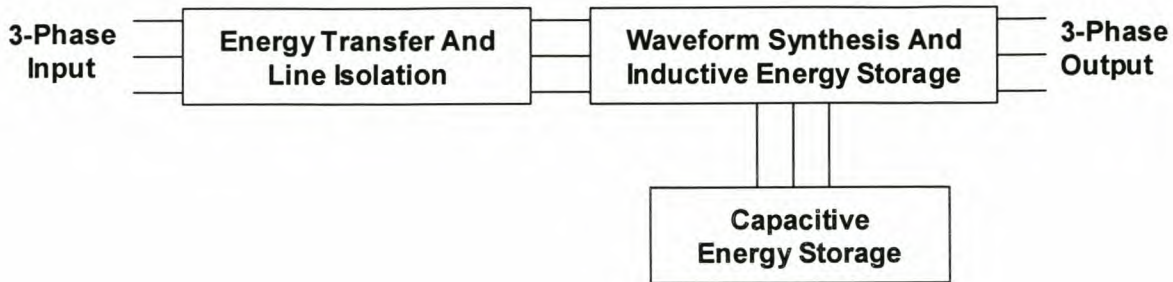


Figure 2.13: Block diagram of magnetic synthesiser.

Energy transfer and line isolation are accomplished through the use of nonlinear chokes. This eliminates problems such as line noise. Staircase waveforms are then generated with a combination of saturated pulse transformers. These pulse transformers also have ferroresonant windings, like CVTs (see ‘Capacitive Energy Storage’ in Figure 2.13) that keep the transformers’ cores saturated for certain deviations in the supply voltage. Finally, the three-phase staircase waveforms are filtered and supplied through a zigzag transformer.

Magnetic synthesisers are generally used for larger loads. The loads must be several kilovoltamperes (kVA) to make these units cost effective. These units are available for loads of 15 – 200 kVA from Liebert Corporation. They are used for large computers and other electronic equipment that is voltage sensitive.

d) Motor-generator sets ([D-8], [D-13])

Motor-generator (M-G) sets come in a wide variety of sizes and configurations and usually utilize flywheels for energy storage (see example in Figure 2.14). They completely decouple the load from the electric power system. Rotational energy in the flywheel provides voltage regulation and voltage support during undervoltage conditions.

One type of M-G set uses an electric motor-driven synchronous generator that can produce a constant 50/60-Hz frequency, regardless of the speed of the machine. It is able to supply a constant output by continually changing the polarity of the rotor's field poles. Thus, each revolution can have a different number of poles than the last one. Constant output is maintained as long as the rotor is spinning at speeds between 3150 and 3600 rpm. Flywheel inertia allows the generator rotor to keep

rotating at speeds above 3150 rpm once power shuts off. The rotor weight generates enough inertia to keep it spinning fast enough to produce 50/60 Hz for about 15 s under full load.

M-G sets have relatively high efficiency and low initial capital cost.

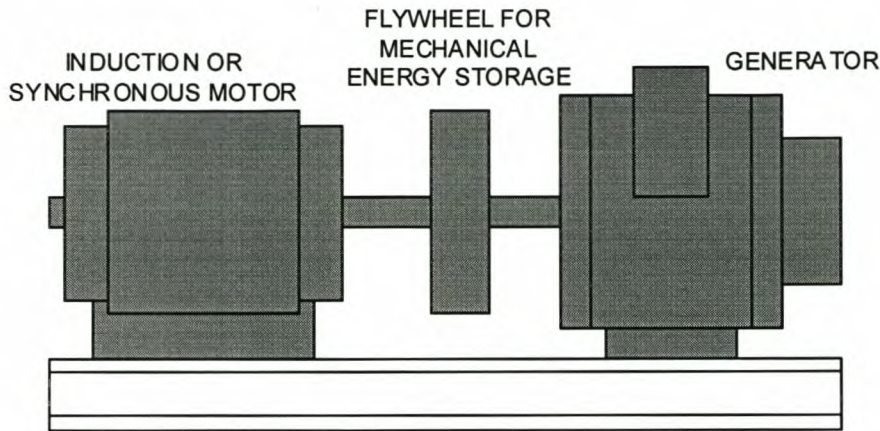


Figure 2.14: *Motor-generator set.*

e) Rotating machines [S-2]

Rainbow Technologies utilises refurbished synchronous machines and series reactors to provide dip compensation. Installations of 35 MVA (33 kV) and 100 MVA (132 kV) are currently in use. The 35MVA “Dip Doctor” consists of a 75 MVA synchronous machine with a 33 kV step-up transformer. The price per kVA for this unit is R286 (in 1995). The 110 MVA system utilises existing turbo alternators together with a 132 kV series reactor. The price of the auxiliary control equipment is R18 per kVA (in 1996).

The “Dip Doctor” does not eliminate dips, but reduces them to levels acceptable to the majority of sensitive plants. Typically the magnitude of dips can be reduced by 50%. The system is mainly suitable for specific types of loads that are not too sensitive to small dips (20% or less) and has limited dynamic response. Typical applications include paper mills, the steel industry, textile and cement mills. It is aimed only at solving a single power-quality problem, namely dip compensation.

f) Conventional UPSs (Uninterruptible Power Supplies)

This type of system is widely used. A basic block diagram representation of this system is shown in Figure 2.15. Most of these systems are based on the so-called double conversion principle. The compensation is done by rectifying the incoming power to produce the DC bus for an inverter in the second stage that generates the output voltage.

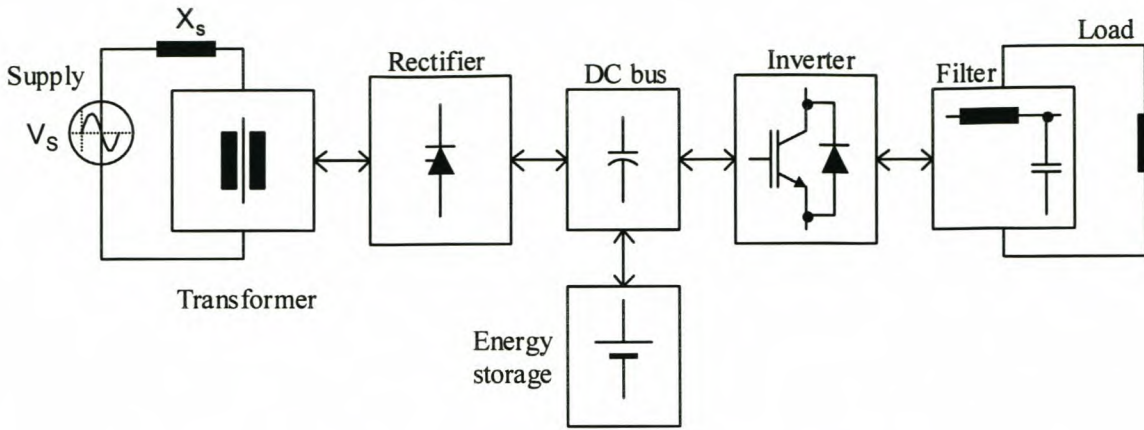


Figure 2.15: Block diagram representation of a conventional UPS.

These systems can be implemented in three configurations [D-8] and compensate for dips and outages. The three configurations are as follows:

- i) *On-line UPS*: Figure 2.16 shows a typical configuration of an on-line UPS. In this design the load is always fed through the UPS. In addition to providing ride through for power outages, an on-line UPS provides very high isolation of the critical load from all power-line disturbances. However, an on-line UPS can be quite expensive and lossy.

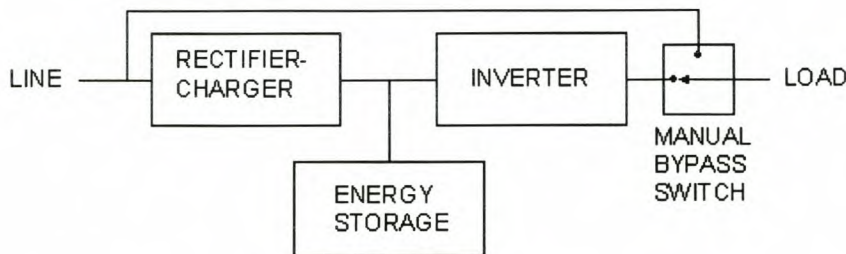


Figure 2.16: Typical configuration of an on-line UPS.

- ii) *Standby UPS*: A standby power supply (Figure 2.17) is sometimes termed "off-line UPS" since the normal line power is used to power the equipment until a disturbance is detected and a solid-state switch (as in the case of the tap-changing transformer) transfers the load to the inverter. A standby power supply typically does not provide any transient protection or voltage regulation as in the case of the on-line UPS.

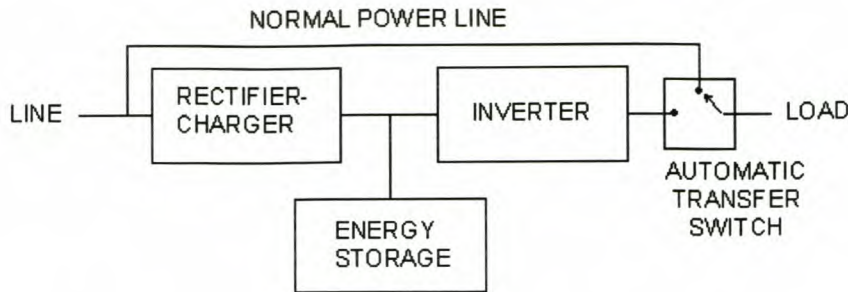


Figure 2.17: Typical configuration of a standby UPS.

iii) *Hybrid UPS*: Similar in design to the stand-by UPS, the hybrid UPS (Figure 2.18) utilises a voltage regulator on the UPS output to provide regulation to the load and momentary ride through when the transfer from normal to UPS supply is made.

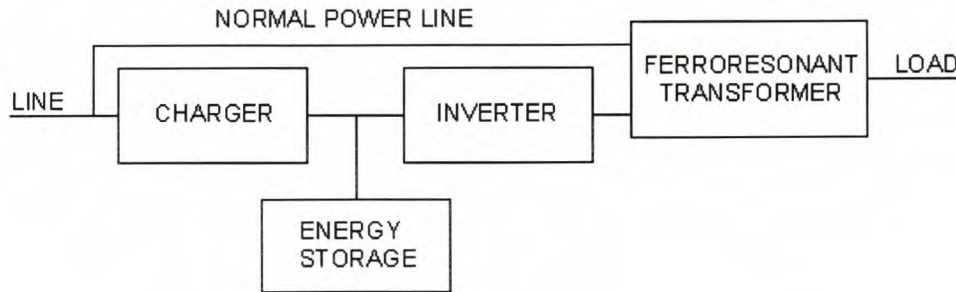


Figure 2.18: Typical configuration of a hybrid UPS.

g) Shunt active filters ([S-6],[S-2])

Figure 2.19 is an example of a shunt active filter and can be used with or without an isolation switch. If the inverter is not isolated from the supply, it can be used to eliminate current harmonics, implement reactive power compensation (also known as STATCON), and balance unbalanced currents. It injects equal compensating currents, opposite in phase, to cancel harmonics and/or reactive components of the nonlinear load current at the point of connection. It can also be used as a static var generator (SVG) in the power system network for stabilising and improving the voltage profile.

When the isolation switch is used, if a dip or outage occurs, the thyristor switch is force-commutated by the inverter, after which the system acts as a UPS. Examples of this type of compensator are the Shunt Silcon Datapower unit [S-2], the Caterpillar UPS and the DUPS (Dynamic Uninterruptible Power Supply) from ABB. Another example is the DPQC (Dynamic Power-Quality Conditioner) that was developed at the University of Stellenbosch, which is

currently being tested on industrial sites with batteries and flywheels as energy storage as part of its pre-industrialised phase. Reference [D-13] also describes the SSD (Superconducting Storage Device) as a shunt compensator in its pre-industrialised phase.

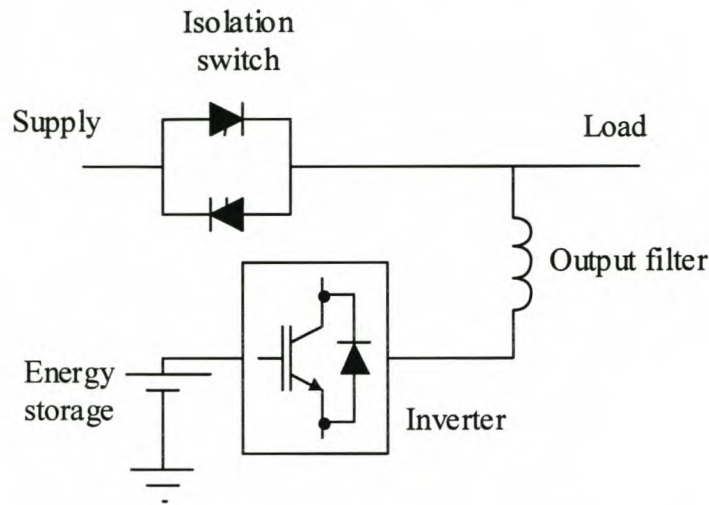


Figure 2.19: *The shunt active filter configuration.*

h) Series active filters ([S-1],[S-2],[S-6])

This type of technology is commercially known as a DVR (Dynamic Voltage Restorer). Figure 2.20 shows the basic block diagram of an active series filter. It is connected before the load in series with the mains, using a matching transformer. This system compensates for dips, outages and flicker and can also perform harmonic isolation. Dip compensation with this topology is implemented by means of an injection transformer in series with the line, which inject the missing voltage. Under dip conditions it injects an extra voltage in series with the line that adds up to the instantaneous voltage to compensate for the sag. This type of compensator's power rating can be reduced to compensate for dips only, giving it an advantage over all the other technologies in terms of cost and energy-storage requirements. As a series compensator it has the disadvantage of having to carry the full load current with the appropriate short circuit protection. A portable 2 MVA DVR with 1 MJ energy storage is available from Westinghouse ([S-2],[S-7]). ABB also produce DVRs. Eskom also has a series compensator with SMES energy storage installed [D-5]. Research on this topology is also still going on at the University of Stellenbosch.

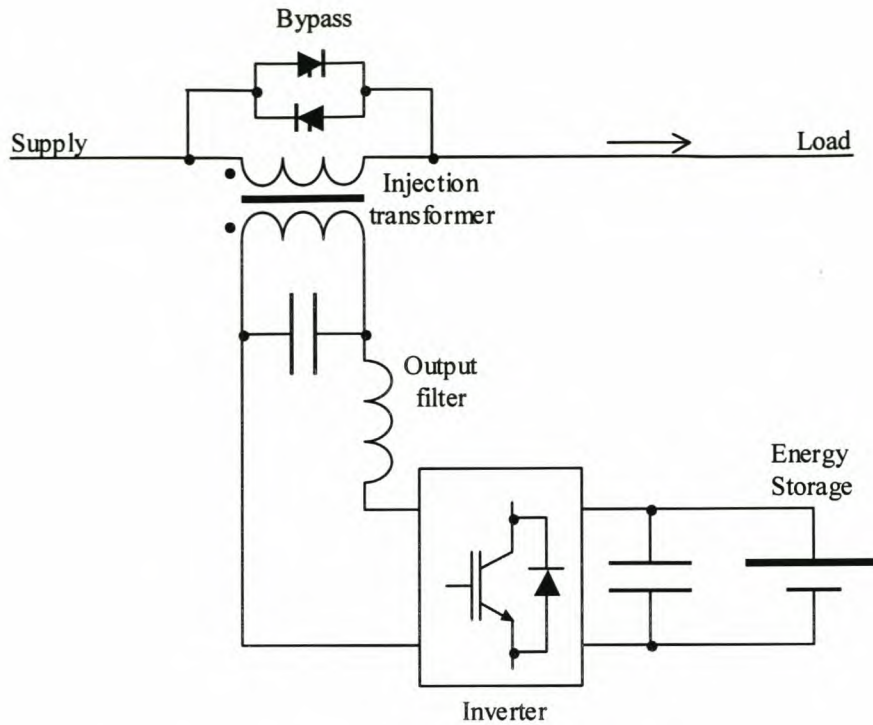


Figure 2.20: Block diagram illustration of the series active filter.

i) Series-shunt active filter ([S-2],[S-6])

This topology is a combination of an active series and an active shunt filter, also known as a unified power-flow conditioner (UPFC) and is illustrated in Figure 2.21. It combines the benefits of the two topologies and serves a variety of purposes. The main advantage is that it optimises network current and load voltage simultaneously. The two DC buses of the series and shunt devices are connected together with the shunt device regulating the DC bus voltage. In this way real power can be injected by the series device.

Using this combination it is possible to compensate for a variety of power-quality and power-flow problems. These include dips, harmonic isolation, harmonic compensation, power factor, voltage regulation, short outages and power-flow balancing.

The unit is also a full FACTS device capable of power-flow control over parallel networks. Figure 2.22 shows two transmission lines with a UPFC in one transmission line. A typical example is a 33kV system fed by dual feeders. The UPFC acts as a phase shifter to balance the power flow between the two lines. With this arrangement one can obtain approximately the same advantages as with an HVDC line but at a fraction of the cost, since not all power is processed through the power electronic converter. The following power-flow control functions can be accomplished with the UPFC :

- Dedicated terminal voltage regulation;

- Dynamic dip compensation;
- Combined series line compensation and terminal voltage control;
- Combined angle regulation and terminal voltage control;
- Combined terminal voltage regulation, series line compensation and angle regulation;
- Harmonic isolation;
- UPS operation during short interruptions, if sufficient energy storage is added;

It is possible for a customer to initially acquire either the series or shunt device and to later upgrade it to a series-shunt device. The power rating of the two units need not be the same and will depend on the type of power-quality solution required. In the UPS mode both units can operate in parallel and support a load of the sum of the individual converter ratings.

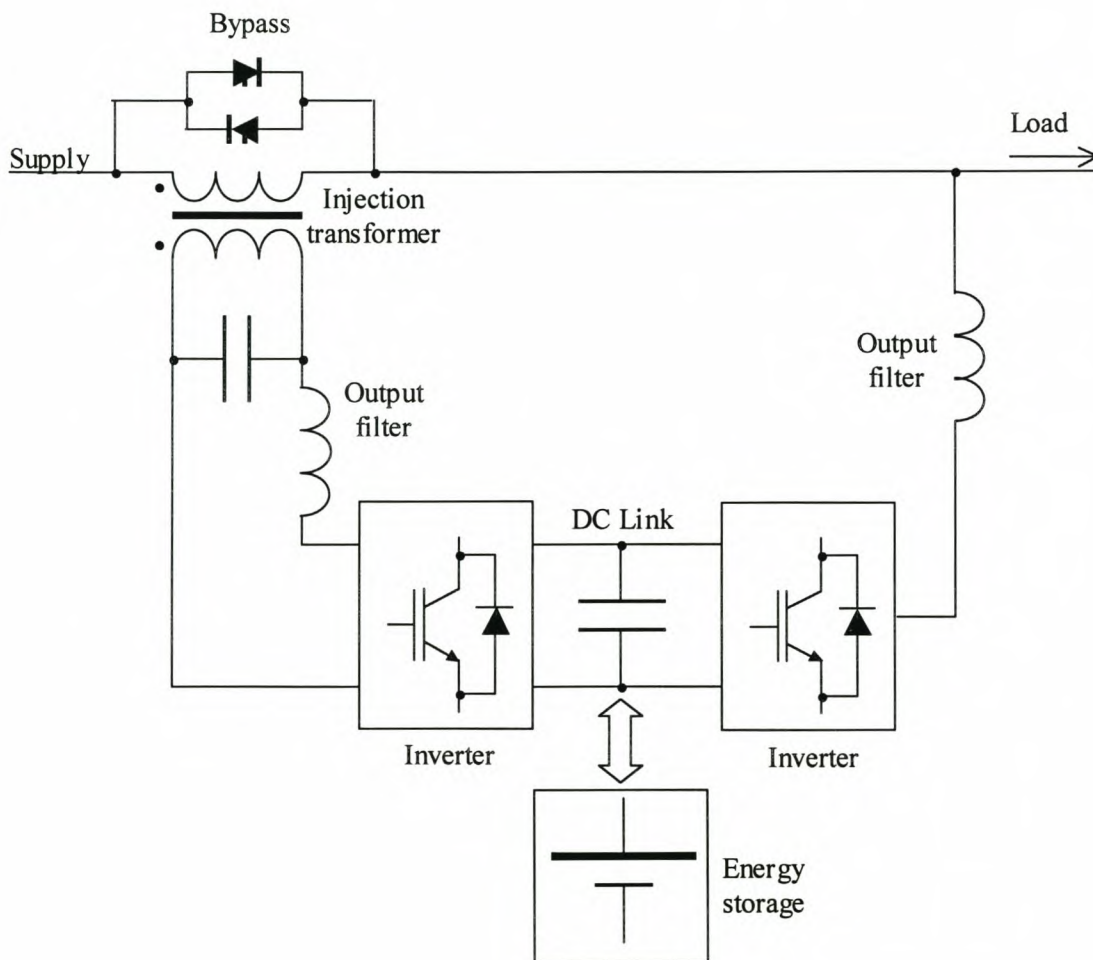


Figure 2.21: Block diagram illustration of the series-shunt active filter.

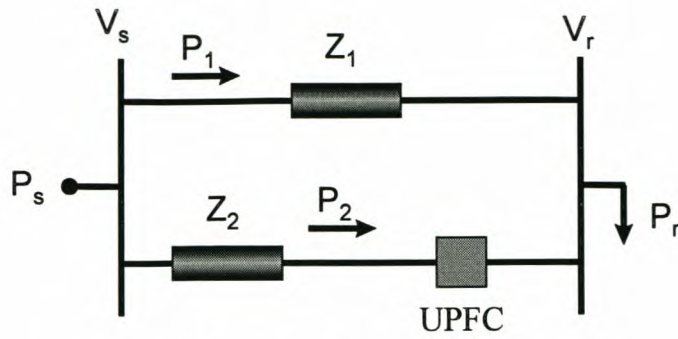


Figure 2.22: UPFC in one transmission line.

j) AC-AC converters ([S-4],[S-5])

Dip compensation is possible with an AC-AC buck or boost rectifier, without energy storage. These topologies are illustrated in Figure 2.23 and Figure 2.24, but they are still in their experimental phase. From the research results of [S-5] the boost converter's (Figure 2.23) output voltage was not very stable during a dip. The buck converter in Figure 2.24 [S-4] had a relatively slow response time of about half a cycle. For the dip that caused an ASD to trip in Figure 2.7, this response might be too slow.

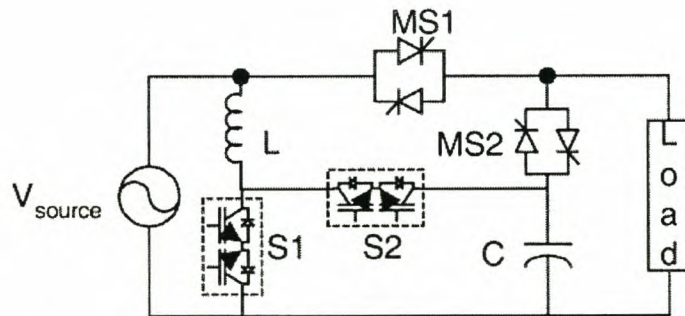


Figure 2.23: Single-phase dip compensator using a boost converter with optional static by-pass switches (MS1, MS2).

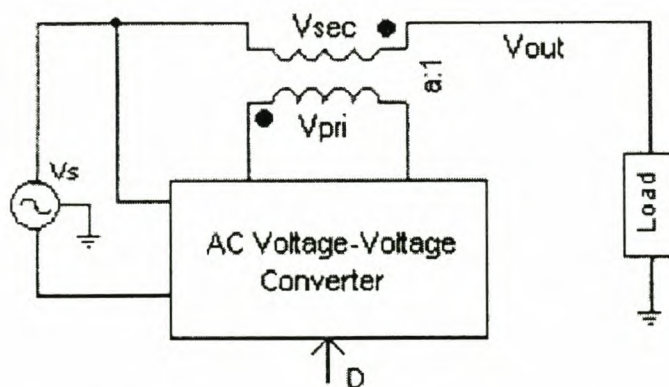


Figure 2.24: Model block diagram of the AC-AC buck converter for dip compensation.

Comparison of power conditioners for dip compensation

Table 2.7 gives an overview of the existing technologies for dip compensation. From the first five technologies, which don't need complex power electronic technology, M-G sets and rotating machines are the most cost-effective solutions with the best performance. UPSs and active filters all have a very good performance, but they also need large transformers, output filter components and energy-storage devices, making them very expensive. The power rating of series active filters can be reduced to compensate for dips up to a certain depth. This is an advantage of series compensation devices, as far as cost effectiveness is concerned. A disadvantage of these devices is that they need special protection against fault currents, because they have to conduct the full load current during compensation. If series active filters are compared with M-G sets and rotating machines, the mechanical solutions' initial cost is much lower. These applications' effectivity, though, is very low, because they will operate for almost 365 days per year, compensating for an approximately 111 dips (see Table 2.6), most of them not longer than 1 second in duration. M-G sets also need lots of maintenance. Series compensation devices, on the other hand, can be implemented with a bypass to operate only when a dip occurs, making their operation cost much cheaper.

Series active filters can be exploited as a cost-effective way of providing dip compensation, but like the other active filter topologies, they use a large transformer (for injection purposes), which has the following disadvantages ([M-10],[M-12],[G-15]):

- They make the system much more expensive. (It is estimated that between 15% to 35% of the total system cost of existing compensators is due to the filter components and transformers);
- They produce about 50% of the total losses of the system;
- They occupy up to 40% of the total system's real estate, which is an excessively large area;
- They cause difficulties in control due to DC magnetising and surge overvoltage problems resulting from saturation of the transformers in transient states;
- They are prone to failure.

Table 2.7: Comparison of power conditioners for voltage dip compensation.

| Technology | Power rating (p.u.) | Transformer | Large filter components | Energy storage components | Other components | Performance | Compensation for other power-quality problems | Commercial/research |
|--------------------------|---------------------|--------------------|-------------------------|---------------------------|----------------------------------|--|---|---------------------|
| Tap-changing transformer | 1.0 | Yes | No | None | Many thyristors | Discrete compensation, slow response | No | Commercial |
| CVT | 4.0 | Yes | No | None | Not of significance | Effective for constant low-power loads | No | Commercial |
| Magnetic synthesiser | 1.0 | Yes, more than one | No | Capacitive storage | Non-linear chokes | Very effective | Yes | Commercial |
| M-G set | 2.0 | No | No | Flywheel | A motor and a generator | Effective for dips of up to at least 6 s | No | Commercial |
| Rotating machine | 1.0 | No | No | No | Series reactor | Reduce dips only | No | Commercial |
| UPS | 2.0 | Yes | Yes | Any type | Many power electronic components | Very effective | Yes | Commercial |
| Shunt active filter | 1.0 | No | Yes | Any type | Power electronic components | Very effective | Yes | Commercial |
| Series active filter | ≤ 1.0 | Yes | Yes | Any type | Power electronic components | Very effective | Yes | Commercial |
| UPFC | > 1.0 | Yes | Yes | Any type | Many power electronic components | Very effective | Yes | Research |
| AC-AC converter | 1.0 | No | Yes | None | Power electronic components | Effective, but limited | No | Research |

These transformers are the main single contributor to the high prices of commercial dip compensators and power-quality devices that range from R1 000 to R2 500 per kVA [S-2]. In order to make series compensation devices more cost effective for voltage dip compensation, possibilities for transformerless series dip compensation are exploited in the next chapter.

Summary

This chapter gave the background on voltage dips. It showed that they are mainly caused by line electrical faults and that this is an increasing concern for the industry, because modern technical equipment is becoming more sensitive to voltage dips. The effects are large financial losses, usually because the process shutdowns caused by voltage dips result in lost production time and damaged products. A lot of measures already exist to compensate for this problem and can be divided into two main groups, namely utility and customer solutions. Customer solutions in the form of power-conditioning equipment seem to be the most effective way to eliminate dips. A lot of power electronic converter technologies (UPS, active filters, AC-AC converters) have been developed for effective dip compensation, but they are very expensive. Transformers are the main single contributors to these systems' costs. The power rating of series compensation devices, like series active filters, can be reduced to compensate for dips of up to a predetermined depth. The possibility of series dip compensation without a transformer can then be exploited as a cost-effective solution for dips.

3. Choosing a cost-effective topology for transformerless series dip compensation

3.1 Introduction

In the previous chapter active filters were discussed as a group of compensation devices that can eliminate dips effectively but which are expensive. It also showed the advantage of series active filters: dips can be compensated for, up to a predetermined depth, at a reduced power rating. The biggest single cost contributor to this compensator is the injection transformer. Although the use of transformers presents advantages, particularly in terms of voltage matching, protection and isolation, the transformer not only increases the cost, but also reduces the overall efficiency of the compensator [M-5]. By eliminating this injection transformer, the compensator's cost can be further reduced.

In this chapter the above-mentioned transformerless compensator is combined with a new range of inverters, called multilevel inverters, in order to develop a cost-effective transformerless series dip compensator. Paragraph 3.2 discusses these topologies. It gives, in fact, an overview of multilevel inverter topologies and compares them to find the most suitable multilevel inverter topology for series dip compensation. Paragraph 3.3 then compares the latter with the single transformerless inverter. The common and unique properties of these topologies are then discussed in order to finally select a cost-effective transformerless series dip compensator.

3.2 Transformerless series dip compensation: comparing the possibilities

At this stage two possible types of transformerless series dip compensators are considered: a conventional inverter with an output filter and one with a multilevel inverter. In this paragraph the two topologies and their advantages and disadvantages are discussed to make the proper selection.

3.2.1 Dip compensation with a single inverter and output filter per phase

If the transformer is eliminated from the series dip compensation device in Figure 2.20 and the output of the filter is connected directly in series with the line, the topology will look like the illustration given in Figure 3.1 for a single phase. This topology can give a more cost-effective solution to dip compensation because of the elimination of the transformer. In this case it won't be possible to use a three-phase inverter as in the case of Figure 2.20. Three single-phase inverters will be used instead due to isolation constraints. Each single-phase inverter will then use its own separate energy storage, which will be a disadvantage compared to the series dip compensator with the transformer.

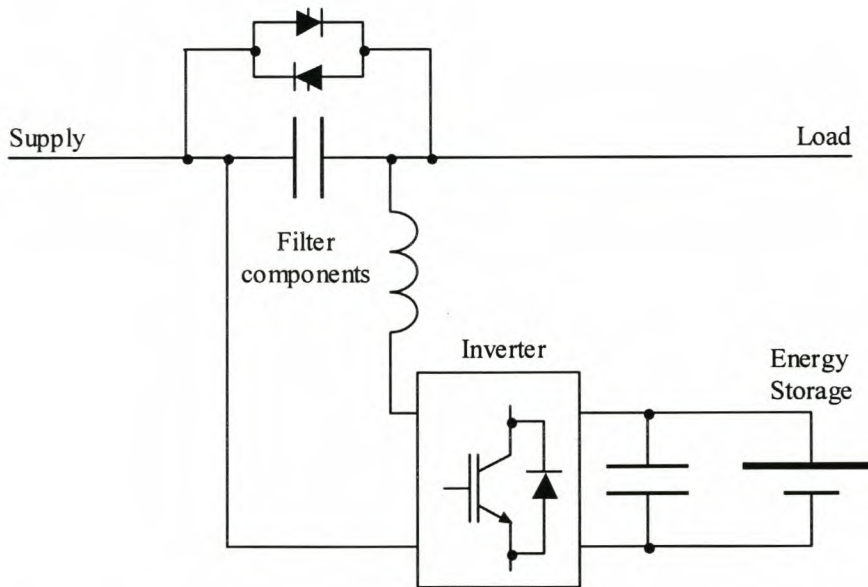


Figure 3.1: *Transformerless series compensation with an output filter.*

3.2.2 Dip compensation with a multilevel cascaded inverter without an output filter

Multilevel inverters, in general, can be categorised into two main groups by their method of coupling to a power line. *Transformer-coupled* multilevel inverters [M-6] are a well-known method and have been implemented in 18- and 48-pulse inverters for battery energy storage, static condenser (STATCON) and Static Var Generator (SVG) applications. An example of a 48-pulse

inverter [M-12] for SVG applications is shown in Figure 3.2. Traditional magnetic coupled multipulse converters typically synthesise the staircase voltage wave by varying transformer turns ratio with complicated zigzag connections. This topology will not be considered due to the large, expensive transformers involved.

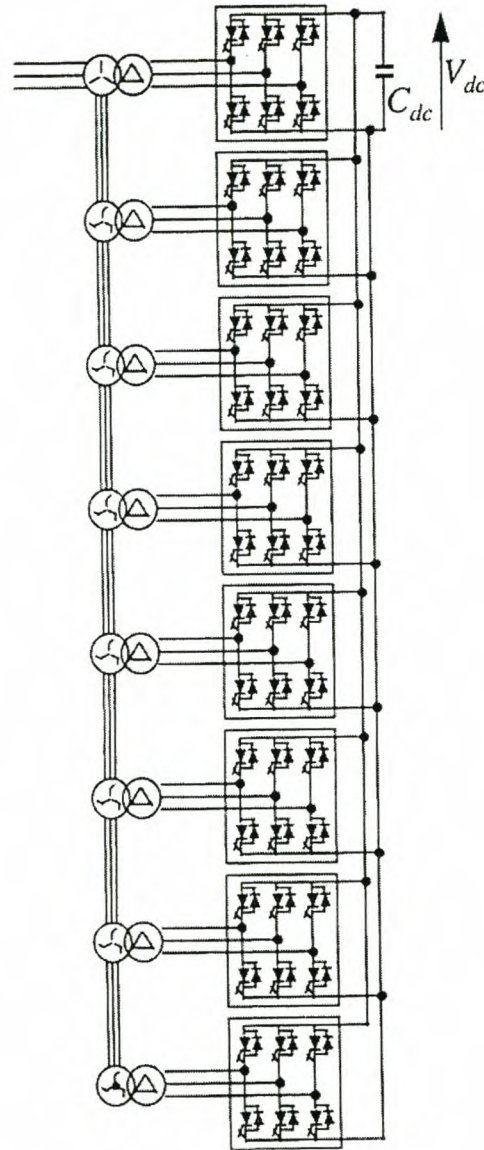


Figure 3.2: Structure of a conventional 48-pulse, transformer-coupled, multilevel inverter.

Direct-coupled multilevel inverters are a relatively new group of inverters that has attracted many researchers' attention [M-12]. A lot of research ([M-1] - [M-13], [C-15]) has been done on the applications and control techniques of these types of inverters. These inverters can reach a high, unfiltered output voltage at multiple voltage levels with reduced harmonics by their own structures without transformers. This property makes it possible to connect these inverters directly in series or

shunt with a power line, because the line provides the inductance needed to interface these inverters with the power system [M-5]. Another virtue of these inverters is their fast dynamic response due to the elimination of large output filter components, which cause delays [M-10].

Normally a multilevel inverter is defined by the amount of voltage levels it can produce in half a cycle [M-6]. Figure 3.3 shows a staircase sine waveform output of a multilevel inverter with 6 voltage levels in half a cycle and 11 voltage levels in total. This inverter is therefore defined as a 6-level inverter. The number of voltage levels depends on the following [M-5]: 1) the injected voltage and current harmonic distortion requirements; 2) the magnitude of the injected voltage required; and 3) the available power switch voltage ratings. The unfiltered output voltage waveform can obtain a relatively low harmonic content, depending on the amount of voltage levels ([M-6],[M-12]). Through the controlling of the switching angles θ_n , certain odd harmonics can be eliminated [M-5]. The staircase sine waveform can then be used for various types of power line compensation. Transformerless series compensation with these multilevel inverters also requires three single-phase units, each with its own energy storage. A brief discussion of the three topologies follows ([M-6],[M-12]).

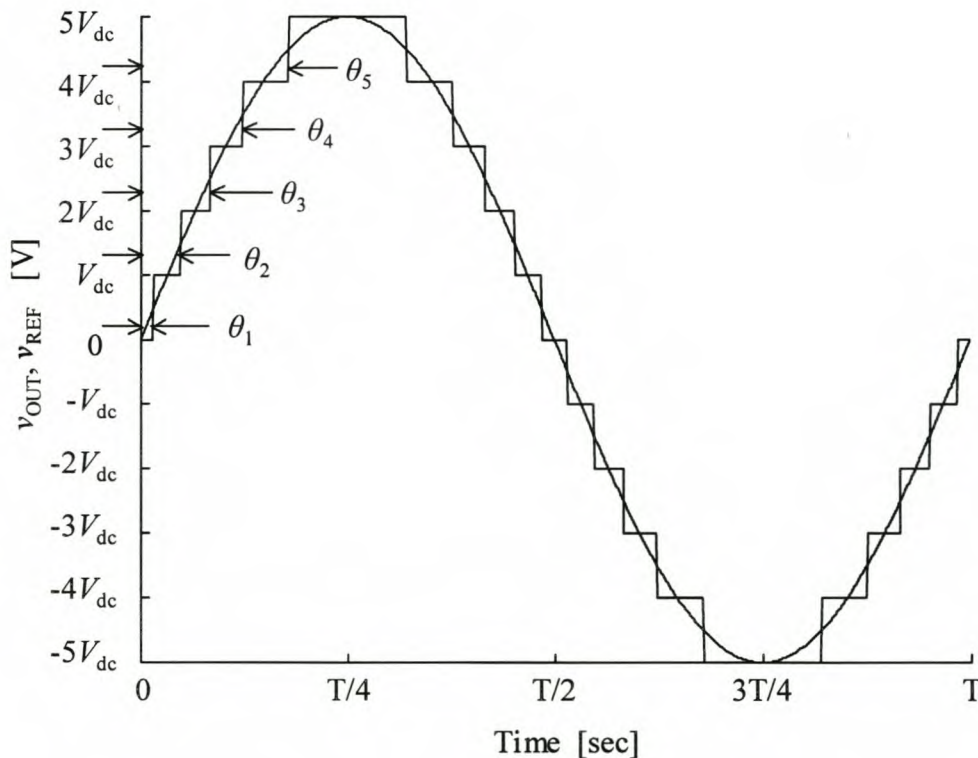


Figure 3.3: Unfiltered staircase sine output waveform of a 6-level inverter.



3.2.2.1 Direct-coupled multilevel inverter topologies

There are basically three existing topologies for this group of inverters [M-6]:

- Diode clamp;
- Flying capacitor; and
- Cascaded inverters.

a) Diode-clamp multilevel converter [M-6]

An m -level diode-clamp inverter typically consists of $m-1$ capacitors on the dc bus and produces m levels of the phase voltage in each half cycle. Figure 3.4 shows a single-phase full-bridge 5-level diode clamp inverter, with a dc bus consisting of four capacitors, C_1 , C_2 , C_3 , and C_4 . For a dc bus voltage $4V_{dc}$, the voltage across each capacitor is V_{dc} , and each device's voltage stress will be limited to one capacitor voltage level, V_{dc} , through clamping diodes. Through different switch state combinations in the upper and lower half of this inverter a staircase sine waveform, with 5 levels in a half cycle, can be generated.

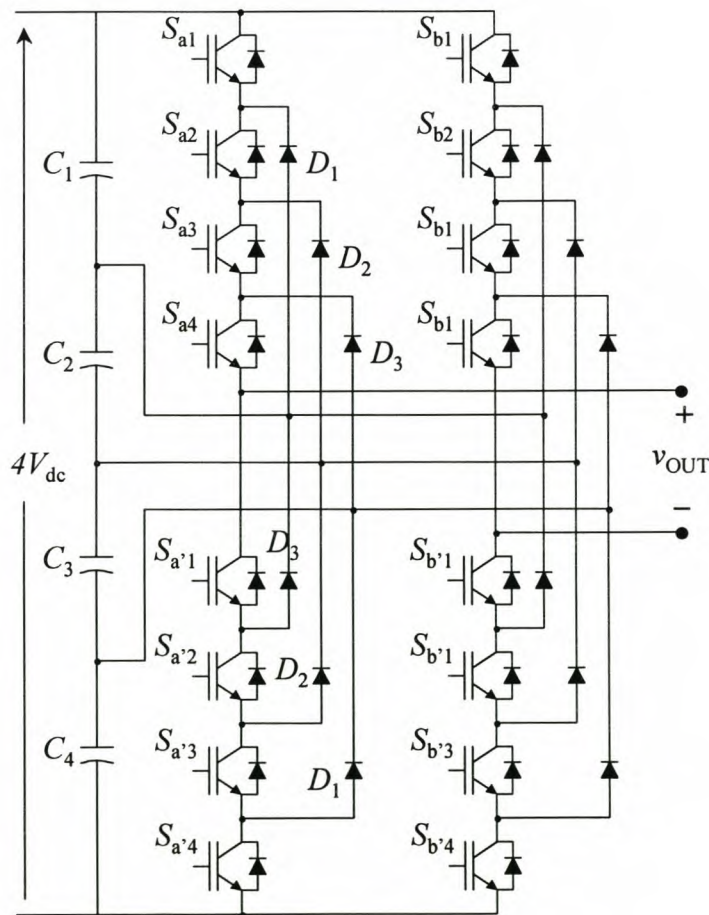


Figure 3.4: A diode-clamp 5-level inverter circuit diagram.

For this 5-level inverter, obviously, D_1 , D_2 and D_3 need to block V_{dc} , $2V_{dc}$, and $3V_{dc}$, respectively, assuming each dc capacitor has the same dc voltage, V_{dc} . When diodes are selected to have the same voltage rating as the main switching devices, D_2 and D_3 comprise two diodes in series and three diodes in series, respectively, to withstand the voltage. Therefore, the number of the additional clamping diodes is equal to $(m-1)*(m-2)$ for a single phase m -level inverter. These clamping diodes not only raise costs, but also cause packaging problems and exhibit parasitic inductances; thus, the number of levels for a multilevel diode-clamped inverter may be limited to seven or nine in practical use.

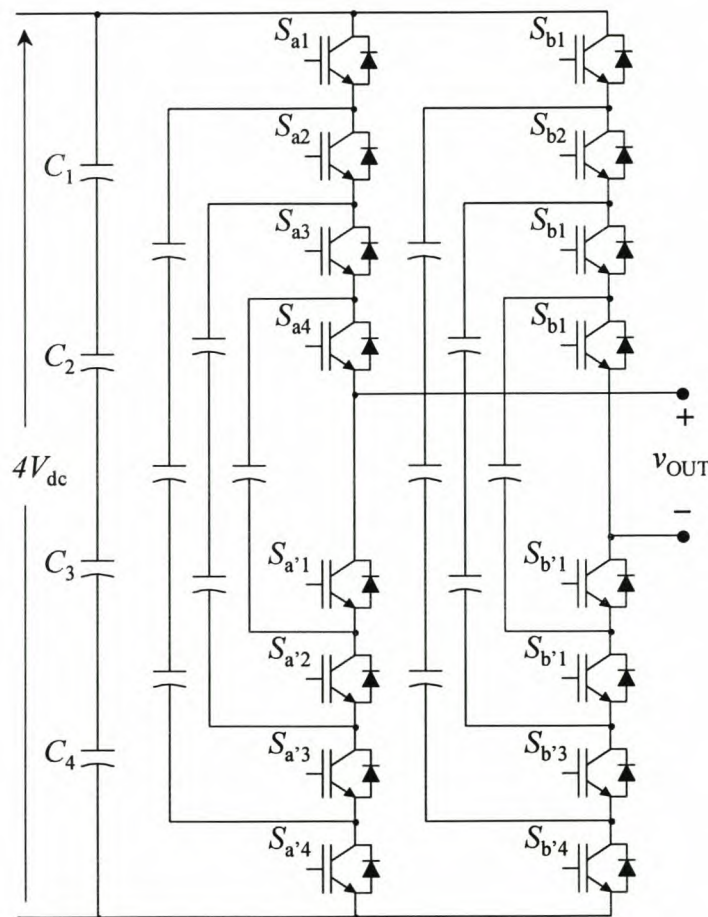


Figure 3.5: Circuit diagram of a flying capacitor-based 5-level single-phase inverter.

b) Flying-capacitor multilevel inverter [M-6]

A relatively new structure, the flying-capacitor multilevel inverter, is supposed to be able to solve the voltage unbalance problem and excessive diode count in multilevel diode clamped inverters. Figure 3.5 shows the configuration of a 5-level flying-capacitor inverter. In this inverter, however, a large number of flying capacitors are needed. The required number of flying capacitors for an m -level single phase inverter, provided that the voltage rating of each capacitor used is the same as the

main power switches, is determined by the formula, $(m-1)*(m-2)/2$ (bus capacitors excluded). With the assumption of the same capacitor voltage rating, an m -level diode clamped inverter only requires its $(m-1)$ bus capacitors. Therefore, the flying capacitor inverter requires a large number of capacitors compared with the conventional inverter. In addition, control is very complicated and higher switching frequency is required to balance each capacitor voltage.

c) Cascaded multilevel inverter [M-6]

Figure 3.6 shows the basic structure of cascaded inverters with separated energy storage components, shown in a single-phase configuration. In this case batteries are used as energy storage, together with DC bus capacitors. The DC bus capacitors are needed for series compensation in order to ensure reactive power flow in both directions on a power line. Each energy storage component is associated with a single-phase full-bridge inverter. The outputs (v_1, v_2, \dots, v_N) of these inverters are connected in series.

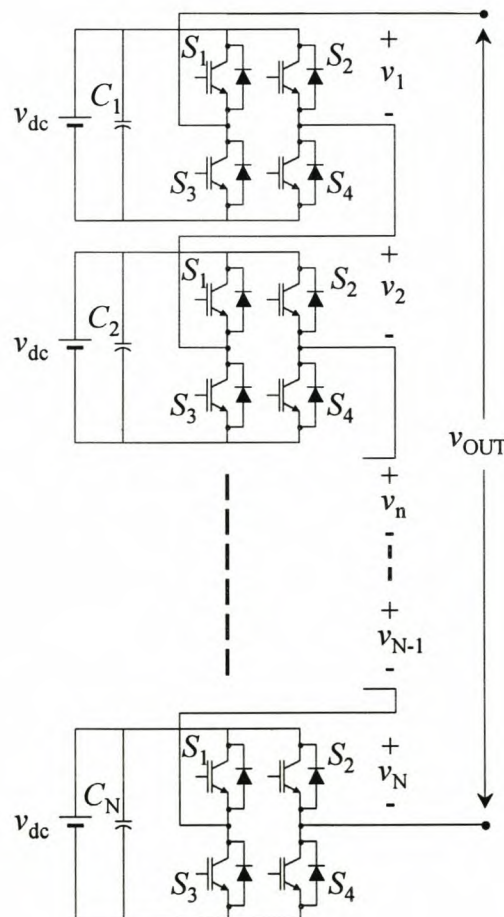


Figure 3.6: Circuit diagram of a multilevel cascaded inverter.

The total phase output voltage is synthesised by the sum of the individual inverters' outputs, i.e. $v_{OUT} = v_1 + v_2 + \dots + v_N$. Each single-phase full-bridge inverter can generate three level outputs, $+V_{dc}$, 0, and $-V_{dc}$. This is made possible by different combinations of the four switching devices (S_1 , S_2 , S_3 and S_4) in each full-bridge inverter. For each inverter turning on S_1 and S_4 yields $v_n = +V_{dc}$. Turning on S_2 and S_3 yields $v_n = -V_{dc}$. By turning on a combination of S_1 and S_2 or S_3 and S_4 , $v_n = 0$. This new multilevel inverter eliminates the excessively large number of (1) bulky transformers required by conventional multipulse inverters, (2) clamping diodes required by multilevel diode-clamped inverters, and (3) flying capacitors required by multilevel flying-capacitor inverters.

3.2.2.2 Applications

There are three main applications for direct-coupled multilevel inverters [M-6].

a) Reactive power compensation

When a multilevel converter draws pure reactive power, the phase voltage and current are 90° apart, and the capacitor charge and discharge can be balanced. Such a converter, when serving for reactive power compensation, is called a static var generator (SVG). The multilevel structure allows the converter to be directly connected to a high-voltage distribution or transmission system without the need of a step-down transformer. Figure 3.7 shows the circuit diagram of a multilevel converter directly connected to a power system for reactive power compensation.

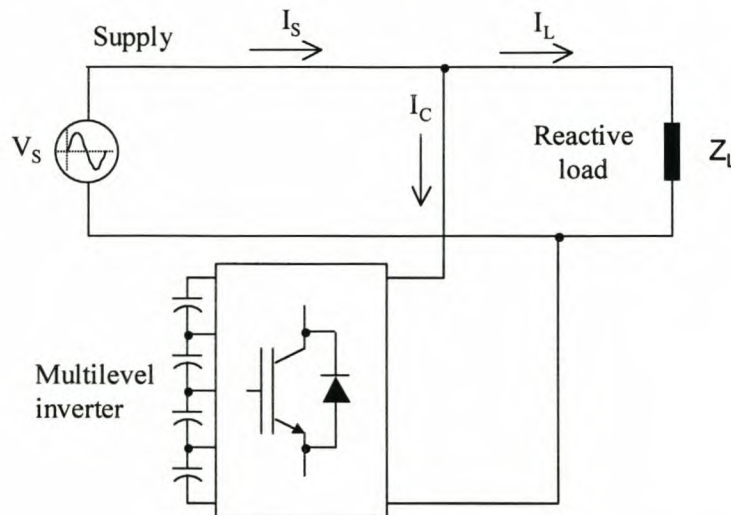


Figure 3.7: Circuit diagram showing a shunt-connected multilevel converter for reactive power compensation.

b) Back-to-back intertie

When interconnecting two diode-clamp multilevel inverters together with a “dc capacitor link,” as shown in Figure 3.8, the left-hand side inverter serves as the rectifier for utility interface, and the right-hand side inverter serves as the inverter to supply the ac load. Each switch remains switching once per fundamental cycle. The result is a well-balanced voltage across each capacitor while maintaining the staircase voltage wave, because the unbalanced capacitor voltages on both sides tend to compensate each other. Such a dc capacitor link is categorised as the “back-to-back intertie”.

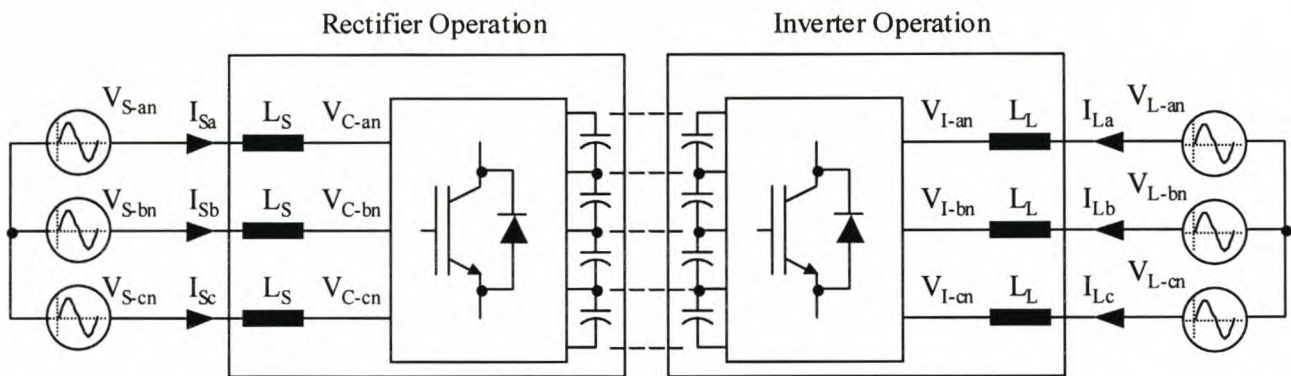


Figure 3.8: General structure of a back-to-back intertie system using two diode-clamp multilevel converters.

The purpose of the back-to-back intertie is to connect two asynchronous systems. It can be treated as 1) a frequency changer, 2) a phase shifter, or 3) a power-flow controller. The power flow between two systems can be controlled bidirectionally.

This system can also be implemented with the flying capacitor topology, but not with the cascaded topology.

c) Utility compatible adjustable speed drives

An ideal utility compatible system require unity power factor, negligible harmonics, no EMI and high efficiency. By extending the application of the back-to-back intertie, the multilevel converter can be used for a utility compatible adjustable speed drive (ASD) with the input from the utility constant frequency ac source and the output to the variable frequency ac load. The major differences, when using the same structure for ASDs and for back-to-back interties, are the control design and the size of the capacitor. Because the ASD needs to operate at different frequencies, the dc link capacitor needs to be well-sized to avoid a large voltage swing under dynamic conditions.

The multilevel inverter-based ASD has a significant advantage over ASDs with a conventional inverter in terms of dV/dt (voltage change rate) and EMI (Electromagnetic Interference). New fast-switching technologies in the latter are now able to switch so fast that the dV/dt is too high. This will result in damaging circulating currents and corona discharge between the winding layers.

3.2.2.3 Comparison of topologies for series compensation ([M-6],[M-12])

The above-mentioned applications for multilevel inverters were used either for shunt compensation (reactive power compensation) or for double power conversion (back-to-back intertie and ASDs). For the application of this thesis multilevel inverters are compared for series compensation, as illustrated in Figure 3.9 for a single phase. This type of compensation also uses three single-phase units of an inverter type due to isolation constraints. The back-to-back thyristor bridge in parallel conducts the line current when there is no dip and it also protect the multilevel inverter from fault currents.

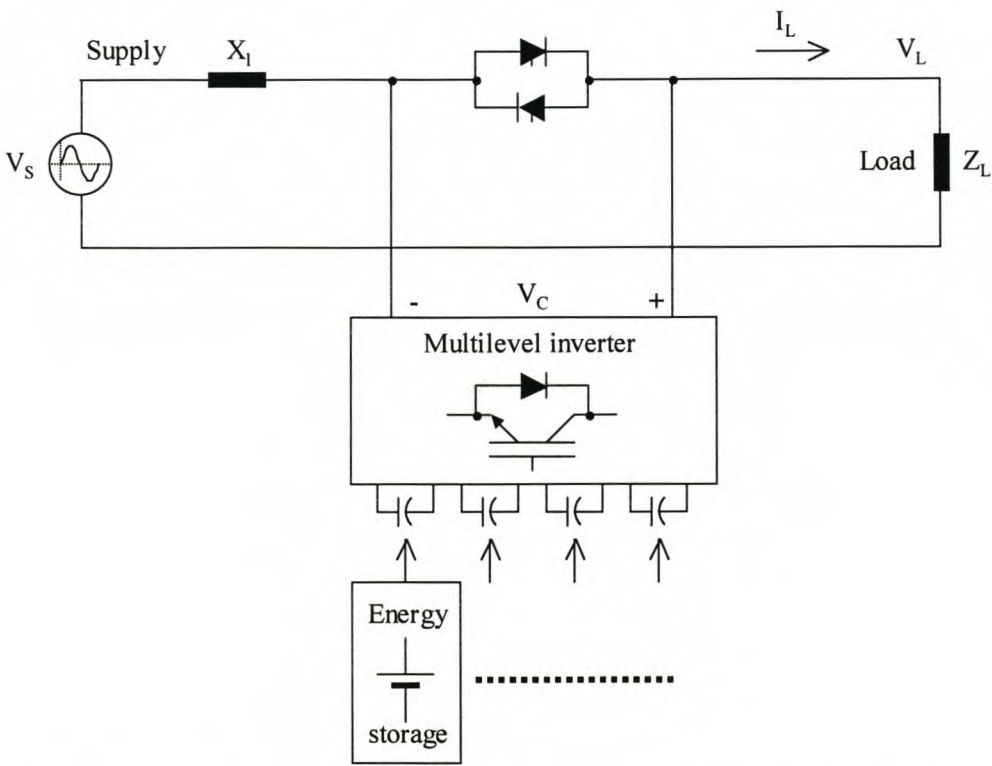


Figure 3.9: *Series dip compensation with a multilevel inverter in one phase.*

Table 3.1 [M-6] shows the component count for each multilevel inverter per phase in terms of the voltage ratings, as stated in 3.2.2.1. This table clearly shows that the cascaded inverter topology has far fewer components due to the elimination of the large numbers of clamping diodes and flying

capacitors. The cascaded inverter structure itself consists of a cascade connection of many single-phase, full-bridge inverter (FBI) units and each bridge is fed with a separate DC source. It therefore does not require voltage balance (sharing) circuits or voltage matching of the switching devices, resulting in a simplified control algorithm. Packaging and layout are also much easier, because of the simplicity of the structure and its modularity. The biggest disadvantage of the cascaded inverter is that each individual inverter needs its own energy storage. This implies that 400 V applications will use battery energy storage, because the other energy storage components only become more cost effective than batteries at higher voltages.

Table 3.1: Comparison of power component requirements per phase among the three topologies.

| Converter type | Diode-clamp | Flying-capacitors | Cascaded-inverters |
|------------------------|-----------------|-------------------|--------------------|
| Main switching devices | $(m-1)*4$ | $(m-1)*4$ | $(m-1)*4$ |
| Main diodes | $(m-1)*4$ | $(m-1)*4$ | $(m-1)*4$ |
| Clamping diodes | $(m-1)*(m-2)*2$ | 0 | 0 |
| DC bus capacitors | $(m-1)$ | $(m-1)$ | $(m-1)$ |
| Balancing capacitors | 0 | $(m-1)*(m-2)$ | 0 |

The cascaded multilevel inverter is therefore chosen as the most applicable multilevel inverter for transformerless series dip compensation.

3.2.3 Comparison of series compensation techniques

In this paragraph the advantages and disadvantages of a single inverter including an output filter, and also that of a direct-coupled multilevel cascaded inverter (as the most suitable multilevel inverter), are discussed and compared for transformerless series dip compensation. These two topologies have several advantages and disadvantages in common and these will be discussed at first.

Common advantages:

- Reduced power rating to compensate for dips up to a predetermined depth;
- Elimination of an injection transformer that will also reduce the cost of the system;

- Low (single inverter with filter) or relatively low (multilevel inverter) harmonic distortion of the injected voltages.

Common disadvantages:

- Can compensate only for dips up to a predetermined depth;
- Switch components need special protection, because they conduct the full line current during a dip;
- Separate energy storage for each phase.

As far as the harmonic distortion of the voltage waveform generated by the multilevel inverter is concerned, a theoretical calculation was made to determine the harmonic content of the compensated load voltage as a function of the depth of the dip. In this calculation a pure sinusoidal supply voltage and a constant dip depth are assumed. If the internal resistance of the batteries and the voltage drop across the MOSFETs are taken into consideration, the voltage steps can be approximated as $V_{dc} = 20$ V.

In [M-13] a formula for the magnitudes of the uneven harmonics was derived from the Fourier Transform of this stepped waveform. This waveform will have no even harmonics if it is symmetrical. The formula for the harmonic amplitudes, normalised with respect to V_{dc} , is as follows for a cascaded inverter with s inverters in cascade:

$$H(n) = \frac{4}{\pi n} [\cos(n\theta_1) + \cos(n\theta_2) + \dots + \cos(n\theta_s)] \frac{\sin(n\omega t)}{n} \quad (3.1)$$

where $n = 1, 3, 5, 7, \dots$

For the method used in this paper the switching angles θ_n ($n = 1, 2, \dots, 5$) can be calculated from the instants when the error voltage V_E reaches the following values: 10, 30, 50, 70 and 90 V. If a phase angle of $\Phi = 0^\circ$ is assumed for the 230 V_{RMS} supply voltage ($V_s = 326 \sin \omega t$), the switching angles can be calculated from the following formula:

$$\theta_n = \sin^{-1} \left(\frac{10 \cdot (2n-1)}{326 \cdot \text{depth}} \right) \quad (3.2)$$

where $n = 1, 2, \dots, 5$ and *depth* is the depth of the dip in %.

The total harmonic distortion (THD) of the injected staircase voltage V_C (see Figure 3.9) and the compensated load voltage V_L were calculated from (3.1) and (3.2) for dips with a depth of 11–30%

at increments of 1%. These values are plotted in Figure 3.10. The THD of the staircase sine waveform V_C is higher at a smaller depth, because it has fewer voltage steps and therefore makes a smaller contribution to the harmonic content of the compensated load voltage. Dips at a larger depth require more voltage steps and result in a smaller THD of V_C , but V_C makes a larger contribution to the total load voltage. The THD of the load voltage therefore remains between 2 and 3%, which is much less than the maximum THD of 8% set by NRS-048 for South African utility standards.

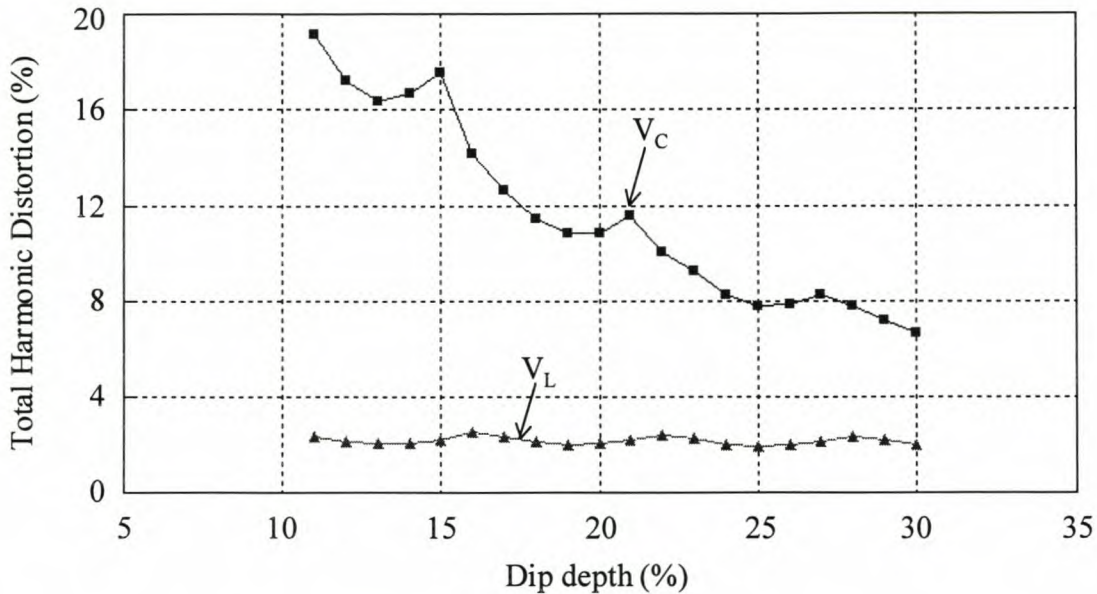


Figure 3.10: Total harmonic distortion (THD) of the injected voltage and the compensated load voltage as a function of the dip depth.

This waveform will also be injected for a very short duration (up to 3 seconds according to the definition in paragraph 2.2). According to NRS 048, harmonics are measured as an average value over 10 min periods. A staircase voltage waveform, injected in series with the power line for a short duration, will therefore have no significant effect on the harmonic standards of the total supply, even if the waveform has a bad harmonic content.

Referring to the last common disadvantage, in the case of the multilevel inverter, each individual inverter has separate energy storage. This will limit the multilevel inverter to batteries as the only cost-effective energy storage at low voltage compensation (400 V line-to-line).

Now that the commonalities have been discussed, the unique properties will be studied in order to determine which of these topologies seems to be preferable, in terms of possibilities, cost and performance that are reasonable.

Table 3.2: *Unique properties of the two topologies.*

| | Single inverter with an output filter | Direct-coupled multilevel cascaded inverter |
|---|--|--|
| Voltage rating | Limited to about 6.5 kV | Limited to the amount of inverters in cascade |
| Large output filter components | Yes | No |
| Packaging and layout | Only one inverter per phase | Multiple inverters per phase (modular) |
| Switching losses | High | Low |
| Control | Continuous, but PWM control of the voltage loop is difficult with varying loads. | Discrete, but fast. |
| Compensation of other power quality problems | Yes | No |

The unique properties of these two topologies are shown in Table 3.2. One of the advantages that will make the multilevel inverter more suitable is that it can be used at very high voltages by just adding more converters in cascade. The single inverter's voltage rating will be limited to the voltage rating of available switching components. Considering switching components with a reasonable bandwidth, it seems that 6.5 kV IGBT's* are the components with the highest voltage rating.

The elimination of the output filter, together with mass production of the multilevel inverter modules, will reduce the multilevel inverter's cost considerably. The modularity makes system design, maintenance and stocking of parts easy. Redundancy is also easily achieved by cascading one more identical H-bridge inverter to the system [M-8].

PWM control of the single inverter, at high frequencies, results in high switching losses. Large heatsinks are therefore needed. In the multilevel inverter's case, the heatsinks can be reduced due to lower switching losses, because each switching component is only switched once in a cycle.

It also seems that the control of the multilevel inverter is simpler than that of the single inverter and this will result in cheaper control technology.

Considering the above facts, the multilevel cascaded inverter is chosen as the more cost-effective option for transformerless series dip compensation.

* EUPEC is currently developing a 6.5 kV IGBT.

Summary

In this chapter the possibilities for transformerless series dip compensation were discussed and compared. A new range of inverters, called multilevel inverters, was also discussed. The multilevel cascaded inverter topology was chosen as the most suitable multilevel inverter for transformerless series dip compensation. This topology eliminates extra clamping diodes and voltage-balancing capacitors which are present in the other topologies. This topology was compared with the single transformerless series inverter for cost-effectiveness. The multilevel cascaded inverter eliminates the output filter, it has lower switching losses than the single inverter and it is modular. These properties give the multilevel inverter the edge in terms of cost effectiveness. This inverter was therefore chosen as a cost-effective topology for transformerless series dip compensation.

4. Hardware design of the single-phase prototype dip compensator

4.1 Introduction

In the previous chapter the multilevel cascaded inverter was chosen as the most suitable topology for series dip compensation with battery energy storage. In this chapter the design of the multilevel inverter, thyristor bypass and supplementary circuits for series dip compensation (see Figure 3.9) are discussed. The main criteria for this design are cost effectiveness and robustness against fault currents at the load side of the dip compensator. Figure 4.1 gives a block diagram illustration of this single-phase dip compensator.

The main part of the hardware design is the multilevel converter that consists of the energy storage, switches, DC bus and driver circuits and is discussed in paragraph 4.2. In the design of the DC bus the robustness of the bus bars against fault currents is verified. Paragraph 4.3 discusses the design of the thyristor bypass for over-current protection. The design of its driver circuit is also included. The design of the over-current detection is discussed in paragraph 4.4. An established DSP control board (PEC 31) is used for the control of the gate signals and is discussed together with the gate signal multiplexer in paragraph 4.5. A summary concludes this chapter.

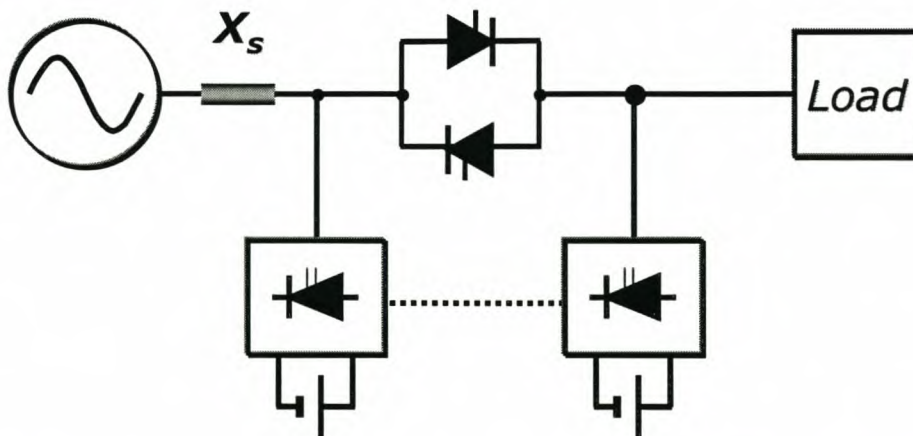


Figure 4.1: Block diagram illustration of the single-phase dip compensator.

4.2 Multilevel cascaded inverter

The dip compensator for this research project must be designed for a single phase of the supply to a typical small industry to compensate for the most general dips. The design specifications for this type of compensator are as follows :

- Line-to-line voltage: 400 V;
- Maximum three phase load: 250 kVA;
- Worst displacement power factor (DPF): $\cos \Phi = 0.85$;
- Maximum depth of dips: 30%;
- Maximum duration of dips: 200 ms.

Eskom, the main utility in South Africa, specified the depth and duration criterion. These specifications are general figures, because they vary from site to site.

To meet these specifications the multilevel converter must be able to inject a staircase sine waveform with the following properties :

- Maximum amplitude: 30 % of the 230 V_{RMS} phase voltage amplitude (approximately 100 V);
- Maximum load current: approximately 360 A_{RMS}.

A multilevel converter, consisting of 5 converters in series, each with a DC bus voltage of 24 V, was decided upon. The extra 20 V in the total DC bus voltage ($24 \times 5 = 120$ V) is to compensate for the voltage losses over the switching components and also the discharge losses due to the internal resistance of the energy storage components.

In the rest of this paragraph, the detailed design of the multilevel converter is discussed.

4.2.1 Energy-storage components

The aim of this part of the design is to find the most cost-effective energy-storage components that will supply the necessary current (360 A_{RMS}) at a low voltage level (24 V) for the maximum time duration (200 ms). A thorough study on energy-storage components for ride-through applications is available in [E-8]. This paper shows that there are mainly four possible types of energy-storage components that can be used in this type of application.

Batteries (Chemical energy storage)

Batteries can store and deliver electrical energy through reversible chemical reactions. Many kinds of batteries have been developed. Lead-acid batteries, which are used in U.P.S. (Uninterruptible

Power Supply) systems, are the most commonly used batteries and hold about two thirds of the current world market [E-8]. These batteries can deliver a relatively constant voltage during discharge, depending on their internal resistance. South African manufacturers of batteries are Willard, UNIROSS, Raylite, First National Batteries and Dixon Batteries.

Ultra/super capacitors (Charge storage)

These capacitors can store very large amounts of electrical charge due to their porous plates (increased plate area). Because $V_C^2 \propto E_C$, a DC-DC converter interface might be necessary to regulate the bus voltage, where V_C defines the capacitor voltage and E_C defines the energy stored in the capacitor. Manufacturers of these capacitors include the following: PowerCache, T/J Technologies, Evans Capacitor Company and Elna America Inc.

Flywheels (Kinetic energy storage)

The principle of flywheels is to use the same machine as a motor and a generator. During discharge they act as a generator to convert kinetic energy to electric energy that is regulated through an active rectifier. Examples of manufacturers of these devices are RPM (Regenerative Power and Motion), Flywheel Energy Systems Inc., Optimal Energy Systems, AFS Trinity Power Corporation, US Flywheel Systems and Urenco.

SMES (Superconducting Magnetic Energy Storage)

In a SMES a high current is kept circulating in a super-conducting coil or magnet until it must be supplied to a load. The fast response and energy efficiency of these devices, because of the low losses, are advantages. The disadvantages of these devices are the overall system cost and the sophisticated refrigeration subsystems that are needed for the cooling of these devices. GE Industrial Systems, American Superconductor and Toshiba are manufacturers of these devices.

Batteries and super-capacitors are the cheapest and the most readily available storage components for the low-voltage levels required in this application. A comparison of these energy-storage devices follows. A thorough survey on energy-storage devices for dip compensation purposes can be found in reference [E-8]. Table 4.1 gives an extract of Table 1 in [E-8].

According to Table 4.1, it seems that batteries have the advantage in all the qualities except for their expected life. Although ultra-capacitors have larger discharge losses and a smaller power density, their maximum discharge time is still long enough for this dip compensator's specifications.

Table 4.1: *Comparison of available batteries and ultra-capacitors for dip compensation systems.*

| System qualities | Ultra-capacitors (Prismatic) | Lead-acid batteries |
|--|---------------------------------|---------------------|
| Maximum duration of discharge (sec) | 5 | 15 |
| Current system retail cost (compare \$/kW) | High | Low |
| Discharge losses (% of rated output power) | 25 | 12 |
| Power density (kW/m ³) | 98 | 173 |
| Expected life (years) | 10-15 | 3-5 |

As cost effectiveness is the biggest factor in this design, the following question arises: if the expected life of both the batteries and ultra-capacitors is taken into account, will a multilevel inverter with batteries still be the cheaper option?

Preliminary designs were done to compare the costs of the multilevel inverter for the most cost-effective available ultra-capacitor and battery. A locally manufactured battery, the **SOLAR 105** from Willard, and an ultra-capacitor (**MAA1915607**) from Evans Capacitor Company were compared in this design.

In the preliminary design the discharge losses and duration of discharge were taken into account. It will be noted that the maximum voltage of the capacitors is higher (30 V) than in the case of the batteries (24 V). This higher voltage is necessary due to a higher discharge rate and higher discharge losses. It can be shown that if the internal resistance and other parameters from the datasheets are taken into account, the discharge of these capacitors, at rated current, will result in a final voltage of 21.5 V after 200 ms for a worst-case scenario (see equation 4.2). An explanation of the cost calculations follows.

Main costs for the multilevel inverter with battery energy storage

Manufacturer: Willard

Product type: Solar 105

Voltage: 12 V

Discharge capability: 105 Ah

Number of batteries per converter for a 24V bus: 2

Cost per battery: R345.00

Total number of batteries for 5 converters: 10

Total cost of batteries: R3450.00

Expected life of the batteries: 3-4 years

Main costs for the multilevel converter with ultra-capacitor energy storage

Manufacturer: Evans Capacitor Company

Product type: MAA1915607

Capacitance: 60 F

Maximum charge voltage: 15 V

A number of parameters are needed in order to calculate the costs in this case.

The total power supplied by the multilevel converter to the load for a 30% dip on a single phase of a 250 kVA three-phase load is as follows :

$$P_{\text{MULTILEVEL}} = (250 \times 10^3)(1/3)(0.3) = 25 \text{ kVA}$$

The total energy supplied to the load for 200 ms will be

$$E_{\text{MULTILEVEL}} = (25 \times 10^3)(0.2) = 5 \text{ kJ}$$

Two of these capacitors in series (for each DC bus) will give a total capacitance of 30 Farad and a maximum charge voltage of 30 V to give the following maximum energy storage per inverter:

$$E_{\text{Cmax}} = \frac{1}{2} CV_{\text{DC}}^2 = 13.5 \text{ kJ} \quad (4.1)$$

It is important to charge the capacitors to this voltage level (30 V), because the voltage of these capacitors decreases faster during discharge than in the case of the batteries. The capacitors also have higher discharge losses. If five converters are used in this multilevel converter and even discharge is assumed, each DC bus will supply 1 kJ of energy to the load. An extra 10% of energy in losses across the switching components is assumed and the discharge losses are also taken into consideration. The final voltage of each DC bus after 200 ms at rated current will then be, from (4.1)

$$V_{\text{DCfinal}} = \sqrt{\frac{2(E_{\text{Cmax}} - 1100 \text{ J})}{C}} - V_{\text{DISCHARGE}} = 21.52 \text{ V} \quad (4.2)$$

*Cost per ultra-capacitor: R2925.00**

Total number of ultra-capacitors for 5 converters: 10

Total cost of ultra-capacitors: R29 250.00

Expected life of the ultra-capacitors: approximately 10-15 years (see reference [E-8])

* Prices converted from dollars at a currency of \$1 = R6.50

The lifetime of the batteries is much shorter. In order to get a more even cost comparison, the cost of the battery design is multiplied by 15/4 resulting in a total cost of R 12 937.50 (compared to R 29 250 in the case of the ultra-capacitors).

It must be remembered that the specified duration of the dip (200 ms) is for the most common dips on power lines in South Africa. For future industrialisation this dip compensator has to be able to compensate for dips of a longer duration. This means that more ultra-capacitors will be needed in this system where batteries have the advantage of a higher power density. If this dip compensator is going to be manufactured in South Africa, importing costs will add to the total costs involved with the ultra-capacitors, while the Solar 105 is a local manufactured battery.

Considering the above facts, the Solar 105 battery is chosen as the most cost-effective energy storage device for this application.

4.2.2 Switching components

These components have to satisfy the following criteria :

- High current rating. They must be able to conduct rated load current ($360 A_{RMS}$), because the compensator operates in series with the power line.
- Low voltage rating. This will be approximately 50 V, because of the low bus voltage (24 V).
- Low losses. They must have a low on-state resistance in order to minimise the voltage loss across them.
- They must be cost effective.

International Rectifier (IR) have quite a lot of Power MOSFETs that meet these criteria. These MOSFETs have very low 'on' resistances ($8-12 m\Omega$) with reasonably high current ratings (81-110 A). By parallelling these MOSFETs, it is possible to get the desired current rating. The fact that MOSFETs can handle extremely high peak currents is another benefit in the design of this series injection device. Table 4.2 shows the available Power MOSFETs from IR with their specific ratings. Two rated values, for parallel combinations of the MOSFETs, in order to conduct the specified current, are also shown: V_{ONmax} represents the maximum total voltage drop across each 'switching component' at rated current ($360 A_{RMS}$) and shows the total rated current for each parallel combination of MOSFETs.

This table shows clearly that the parallel combination of the IRF1010E is the most cost effective. If ten of these MOSFETs are connected in parallel, it will be able to conduct currents of up to 810 A at $T_C = 25^\circ\text{C}$. For the given current rating, this parallel combination of MOSFETs will have a maximum on-state voltage of 0.61 V. The price of the MOSFETS per inverter will be only *R 260.00. These components are also readily available from Advanced Product Tech Ltd.

It can be argued that the MOSFETs in parallel will not conduct the current equally, because the on-state resistance values may have a small tolerance. According to par. 22-6-3 of reference [G-10], MOSFETs can be paralleled easily, because of the positive temperature coefficient of their on-state resistance. This means that if one MOSFET conducts more current than the others, an increase in temperature along with its on-state resistance will result in a decrease in its share of the current. This effect is called “thermal stabilisation” and demonstrates another advantage of MOSFETs. Switching components in parallel is not a new concept. Paralleling of GTOs in a diode-clamped multilevel inverter, for STATCOM purposes, was exploited in reference [M-2] in order to improve the control of a STATCOM.

Table 4.2: *Comparison of the MOSFETS and all the possible combinations.*

| Power Mosfets from International Rectifier | | | | | | | | | |
|---|------------------|---------------------------|--------------|--------------|--------------------------|------------------|--------------------|------------------|-----------------------------|
| Component | V_{DSS} [V] | R_{DS} (on) [ohm] | I_D [A] | P_D [W] | Price per unit [R] | Mosfets in // | V_{ONmax} [V] | $I_{D//}$ [A] | Cost per inverter [R] |
| IRF1010E | 60 | 0.012 | 81 | 150 | 6.50 | 10 | 0.61 | 810 | 260.00 |
| IRF3205S | 60 | 0.008 | 110 | 200 | 26.30 | 6 | 0.68 | 660 | 631.20 |
| IRL2505 | 60 | 0.008 | 104 | 200 | 24.41 | 6 | 0.68 | 624 | 585.84 |
| IRFP064N | 60 | 0.008 | 110 | 150 | 13.60 | 6 | 0.68 | 660 | 326.40 |
| IRF3205L | 60 | 0.008 | 110 | 200 | 26.30 | 6 | 0.68 | 660 | 631.20 |

4.2.3 DC Bus

This part of the design consists of the DC bus capacitors and also the busbars.

* Prices obtained at the beginning of 1999. The latest available price of the IRF1010E, before submission of this thesis, was R10.50 per unit. This will give a total price of R420.00 per inverter.

4.2.3.1 Bus capacitors

It has already been stated that this dip compensator must be able to compensate for reactive loads with a worst displacement power factor (DPF) of $\cos \Phi = 0.85$. Bus capacitors are important to keep the bus voltage stable and also to absorb the reactive current during dip compensation on reactive loads. These capacitors must be designed for a low voltage (approximately 50 V) and for the necessary ripple current rating.

Two papers on multilevel cascaded inverters ([M-12], [M-8]), which discuss the design of the bus capacitors, are available. These papers discuss this design for var shunt compensation purposes only. Another way had to be found to design the DC bus capacitors for series compensation with a multilevel cascaded inverter with battery energy storage.

Figure 4.2 illustrates a worst-case scenario where an individual inverter has a voltage step at its output for the whole duration of each half cycle where the DPF is $\cos \Phi = 0.85$. This scenario will definitely causes the load current to flow into the DC bus of an inverter. The capacitors have to be designed to absorb this ripple current and also reduce the voltage fluctuations on the DC bus.

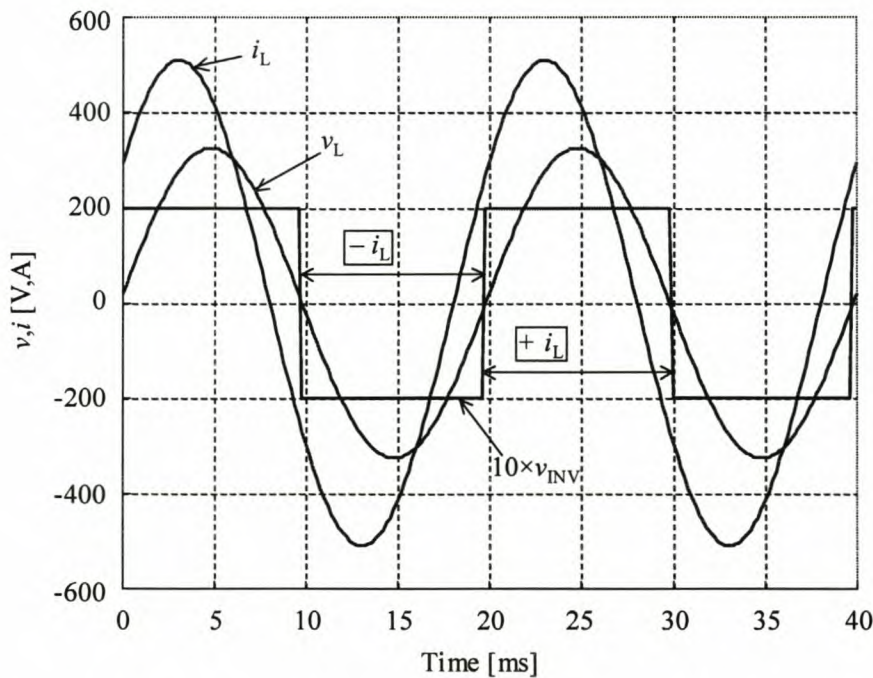


Figure 4.2: Illustration of a worst-case scenario for the capacitor ripple current when the displacement power factor is equal to 0.85.

An equivalent circuit of the scenario illustrated in Figure 4.2 is shown in Figure 4.3 when the inverter has a positive voltage step at its output. The battery is represented by an ideal voltage

source, V_b , and an internal resistance, R . C represents the DC bus capacitance and $i_L = I \sin(\omega t + \Phi)$ represents the load current.

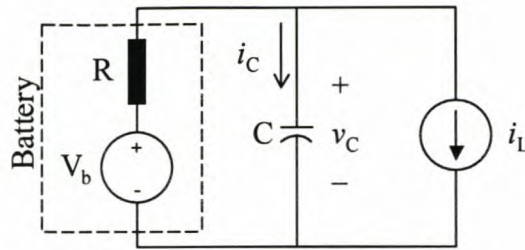


Figure 4.3: *Equivalent circuit of an inverter for the scenario in Figure 4.2 for a positive voltage step at the output.*

A simulation in Simplorer is used to determine the value of the DC bus capacitance for the optimum capacitor ripple current, i_C , and DC voltage deviation, Δv_C . In this simulation the following values are used:

- $V_b = 24 \text{ V}$
- $R = 15 \text{ m}\Omega$
- $C = 200 \text{ mF}$
- $I = \sqrt{2} \times 360 \text{ A}_{\text{RMS}} = 510 \text{ A}_p$ and $\phi = \cos^{-1} 0.85$ for $i_L = I \sin(\omega t + \Phi)$.

Figure 4.4 shows the simulated waveforms of the load and the capacitor ripple current from the simulation in Simplorer. The r.m.s. value of the ripple current is about 210 A. The deviation in the capacitor voltage v_C is about $\pm 10\%$ around its average value, which drops to about 20 V when the inverter supplies current to the load. The internal resistance of the battery causes this drop in the average DC bus voltage.

If the DC bus capacitance is increased, the deviation in the DC bus voltage will decrease, but the r.m.s. ripple current value will increase. The opposite will occur if the capacitance is decreased. This value of $C = 200 \text{ mF}$ is chosen as the optimal value for the DC bus.

After considering a lot of parallel combinations of low-voltage capacitors with their respective ripple current ratings the 1 mF, 63 V USL electrolytic capacitor of Samsung was chosen as the most cost-effective option. Its rated ripple current is $1.891 \text{ A}_{\text{RMS}}$, resulting in a total ripple current of $378 \text{ A}_{\text{RMS}}$ for 200 capacitors in parallel. The cost of each capacitor is R2.02 resulting in a total cost of R404.00 for each DC bus.

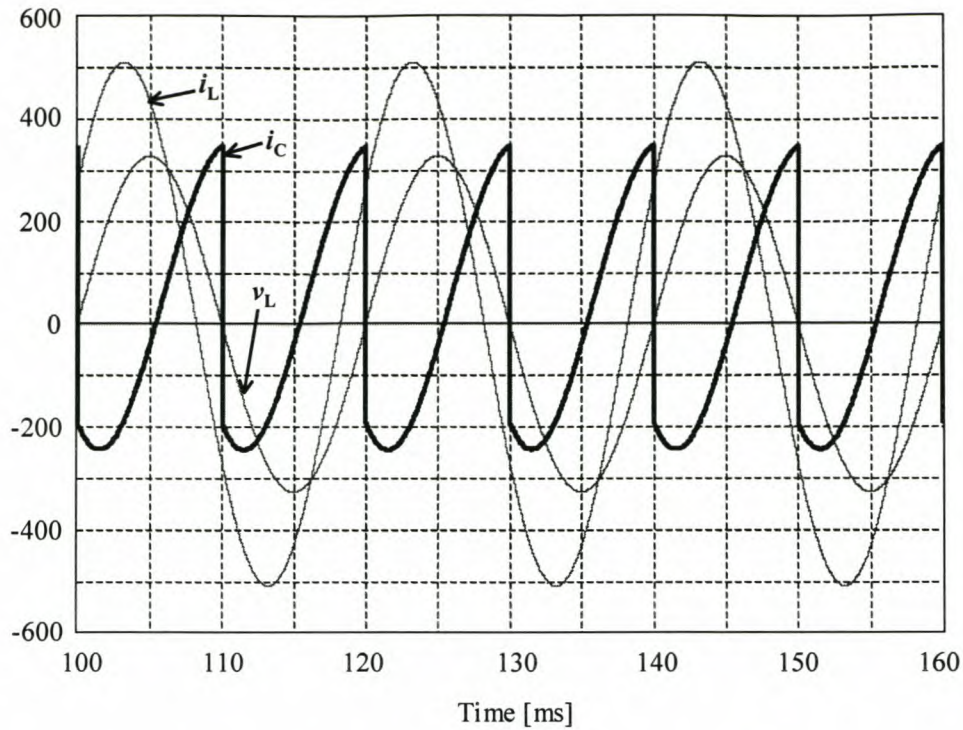


Figure 4.4: Simulation of the capacitor ripple current i_C , together with the load current i_L and load voltage v_L .

4.2.3.2 Bus bars and heatsinks

This part of the design is very difficult, because the type of switching components and DC bus capacitors that are used don't have screw terminals like the types that are normally used at this power rating. This calls for a unique design of the bus bars. The following requirements also have to be met:

- Each switch consists of 10 MOSFETs in parallel that all have to be mounted on the bus bars (see paragraph 4.2.2).
- The spacing between the bus bars in the region of the MOSFETs should be kept to a minimum in order to reduce unnecessary stray inductances that will increase the over-voltages across the MOSFETs at high currents.
- The bus bars should also serve as heatsinks in order to absorb the heat that is generated in the MOSFETs during a dip when they are switched.
- It should also be able to conduct fault currents for the short durations that it might occur.
- For practical purposes, the bus bars must fit on top of the batteries.

The third requirement is possible because the MOSFETs only switch for short durations (up to 200 ms) at a very low switching frequency (line frequency: $f = 50$ Hz). Calculations that prove this point follow.

In order to minimise losses, the MOSFETs are controlled to conduct for only half a cycle in the steady state part of the dip (see Chapter 5 on control). The calculations of the losses (from eq. 2-6 and 2-7 of paragraph 2-4 in [G-10]) below are for only one MOSFET and thus for a tenth of the load current ($I_L/10$).

Conducting losses:

$$P_{on} = \left(\frac{I_L}{10} \right)^2 R_{on} \frac{t_{on}}{T_s} = 7.8 \text{ W}, \quad (4.1)$$

where I_L is the load current at 360 A_{RMS}, $R_{on} = 12 \text{ m}\Omega$ and $\frac{t_{on}}{T_s} = 0.5$ for the reasons stated above.

Switching losses:

$$P_s = \frac{1}{2} V_{dc} \frac{I_L}{10} f_s (t_{c(on)} + t_{c(off)}) = 0.043 \text{ W}, \quad (4.2)$$

where $t_{c(on)} = 1 \text{ }\mu\text{s}$

$t_{c(off)} = 1 \text{ }\mu\text{s}$ (see paragraph 4.3.4),

V_{dc} is the bus voltage (24 V) and f_s is the switching frequency (50 Hz). Because of the low switching frequency, these losses is negligible.

Total losses:

$$P_t = P_{on} + P_s = 7.8 \text{ W} \quad (4.3)$$

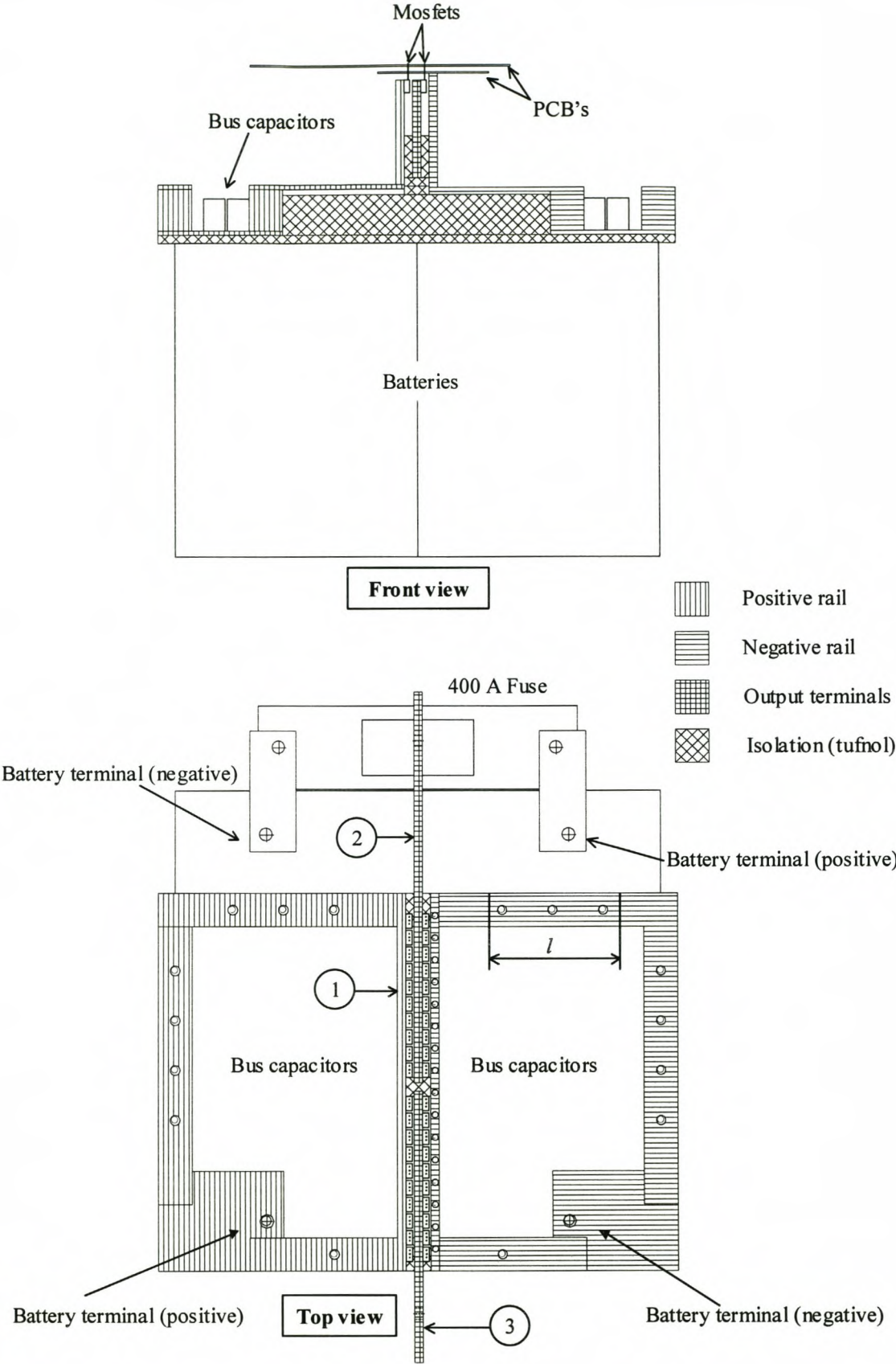


Figure 4.5: Construction of the busbars.

With $R_{\theta JC} + R_{\theta CS} = 1.4 \text{ } ^\circ\text{C/W}$, these losses will result in a junction temperature rise of about 11°C for each MOSFET.

The heatsink of each MOSFET is connected to the drain. If half of the MOSFETs (top 2 switches) are mounted on the positive rail (bus bar 1 – see Figure 4.6) of the bus bars and the other half are mounted on the output terminals (bus bars 2 and 3) of the H-bridge inverter, the bus bar in the former case will have to absorb $20 \times 7.8 = 156 \text{ W}$ and 78 W in the latter case, both for a duration of 200 ms .

Figure 4.5 shows the design for the construction of the bus bars. Both the top view and the front view show where the MOSFETs are mounted on the bus bars. Two PCBs are mounted on top of the MOSFETs. The bottom PCB connects the source of the top switch to the drain of the bottom switch in each phase arm. The top PCB contains the driver circuits and the isolated power supply. In the top view of the bus bars the PCBs are excluded. A 400 A fuse is included in series with the batteries to protect them from short-circuit currents.

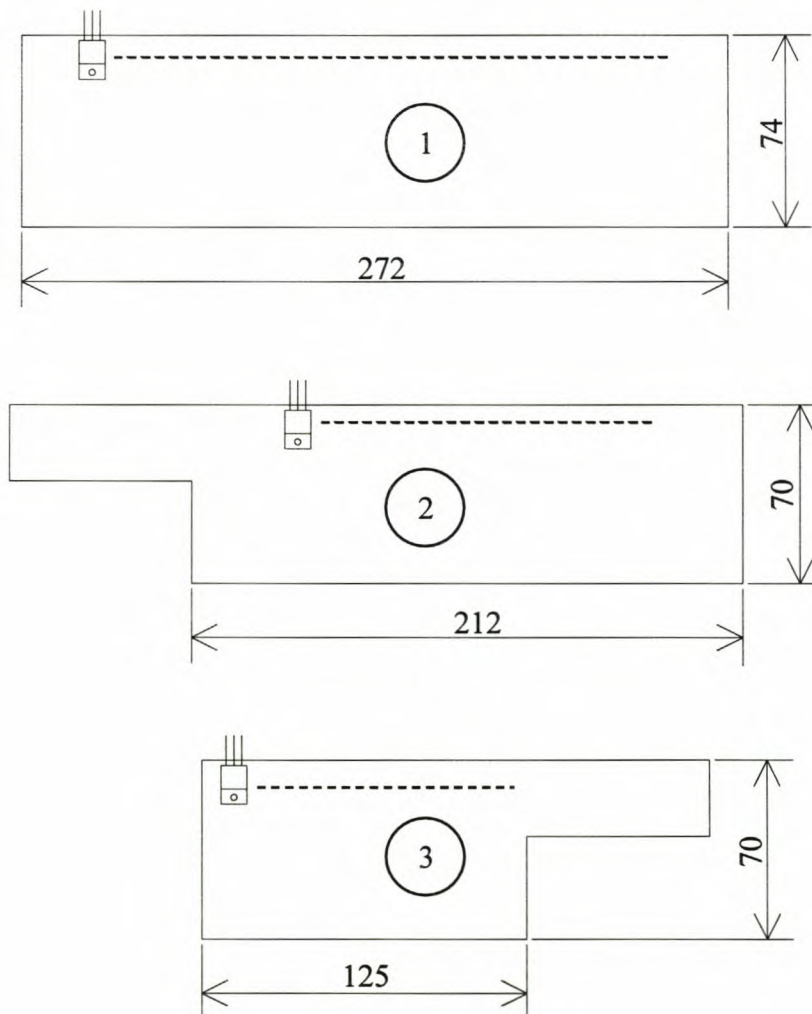


Figure 4.6: Bus bars on which the MOSFETs are mounted on.

Figure 4.6 shows the parts of these copper busbars on which the MOSFETs are mounted. Part 1 in Figure 4.6 represents the positive rail and parts 2 and 3 represent the output terminals of the inverter. This is so because the heatsink terminal of the MOSFETs is connected to the drain. 20 MOSFETs will therefore be mounted on part 1 and 10 MOSFETs will be mounted on parts 2 and 3 each.

Parts 1 to 3 have to absorb the heat that is generated by the MOSFETs when they switch during a dip. The temperature rise of these parts during a dip has to be calculated with equation 4.4 (from eq. 20.4 in [G-13]) in order to prove that this is the case. In these calculations the effects of convection and radiation are neglected.

$$\Delta T = \frac{Q}{mc}, \quad (4.4)$$

where $\Delta T \equiv$ temperature rise in the copper

$Q \equiv$ energy dissipated in the MOSFETs

$m \equiv$ mass of the copper

$c \equiv$ heat capacity of the copper (387 J/kg°C).

The energy (Q) that is dissipated in the MOSFETs for a 500 ms dip for each copper part is calculated as follows :

$$Q_1 = (7.8 \text{ W})(20)(500 \text{ ms}) = 78.0 \text{ J}$$

$$Q_{2,3} = Q_1/2 = 39.0 \text{ J}$$

The mass (m) of each copper part can be calculated with the following equation :

$$m = \rho V \quad (4.5)$$

where $\rho_{\text{COPPER}} = 8.93 \times 10^3 \text{ kg/m}^3$ (mass density). The mass of each copper part is then as follows:

$$m_1 = 1.078 \text{ kg}$$

$$m_2 = 0.795 \text{ kg}$$

$$m_3 = 0.469 \text{ kg.}$$

From eq. 4.4 the temperature rise in each copper part (assuming that all the dissipated power in the MOSFETs is transferred to the copper) is:

$$\Delta T_1 = 0.187^\circ\text{C}$$

$$\Delta T_2 = 0.127^\circ\text{C}$$

$$\Delta T_3 = 0.215^\circ\text{C}$$

These values show that the temperature rise in all the copper parts is almost negligible for a 500 ms dip that is of an even longer duration than the specified 200 ms.

The ability of the bus bars to conduct a fault current for a very short while also needs to be verified. According to Eskom the fault level on any line is normally more or less ten to twenty times the rated current. This dip compensator is designed for a fault current of twenty times the rated current ($7.2 \text{ kA}_{\text{RMS}} = 20 \times 360 \text{ A}_{\text{RMS}}$). The maximum temperature rise in the bus bars, as in the previous case, therefore has to be calculated for this current. This is done by taking just a part of the bus bars with the smallest conducting surface, as a sample, as marked in Figure 4.5. This part has a conducting surface of $A = 3 \text{ mm} \times 24 \text{ mm}$ and a length of $l = 100 \text{ mm}$, for instance. The resistance of this piece of copper must be calculated in order to determine the temperature rise resulting from the fault current. It is a well-known fact that, although the current distribution in a conductor cross-section is uniform with a DC current, this is not the case for AC currents. This non-uniformity of the current increases with increasing frequency and the current tends to crowd toward the conductor surface, with smaller current density at the conductor centre, resulting in a higher resistance at higher frequencies. This phenomenon is called the *skin effect* [G-6]. According to [G-6], the ac resistance of conductors like copper is at most a few percent points higher than the DC resistance. The skin effect is therefore neglected in this calculation. From the following equation

$$R = \rho \frac{l}{A} \quad (\text{from eq. 27.10 in [G-13]}), \quad (4.6)$$

where $\rho_{\text{COPPER}} = 1.7 \times 10^{-8} \Omega \cdot \text{m}$ (resistivity), the resistance of this piece of copper is calculated as $R = 23.6 \times 10^{-6} \Omega$. The power dissipated in this piece of copper for the previously stated current is then $P = I^2 R = 1.22 \text{ kW}$.

The breaking time of the NS630N circuit breaker in the laboratory for these type of currents is less than 60ms. If the time duration of the fault current is assumed as 60 ms, the temperature rise in this piece of copper, according to (4.4) and (4.5), will be $\Delta T = 2.94^\circ\text{C}$. This is a very small temperature rise for such a large current and this value therefore verifies the fact that the bus bars are fully capable of conducting fault currents (melting point of copper: 1083°C).

4.2.4 Power supply and driver circuits for MOSFETs

A block diagram representation of these circuits is shown in Figure 4.7. (The complete circuit diagrams of these circuits and the rest of the new circuits are available in Appendix B.)

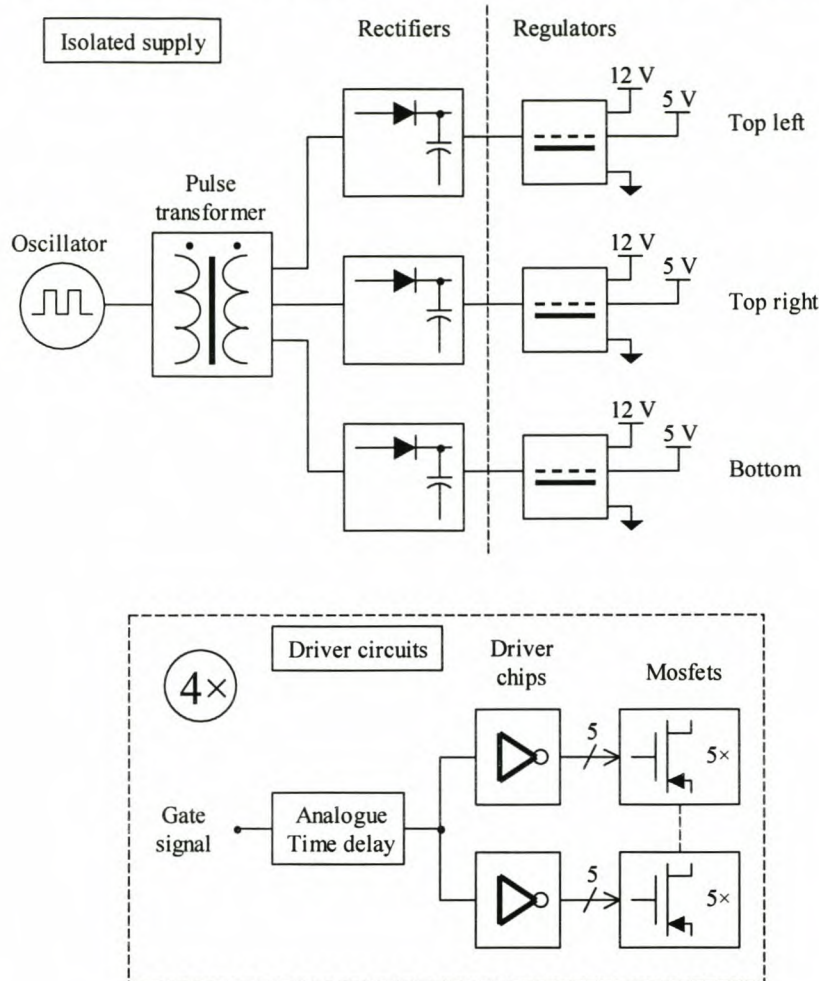


Figure 4.7: Block diagram of the isolated supply and driver circuits of the MOSFETs.

Power supply

Each individual converter needs an isolated power supply with one ground reference for the two bottom switches and a different ground reference for the each of the two top switches. It consists of a 50 kHz oscillator, with its output on the primary side of a pulse transformer, and three secondary windings that supply the necessary voltage for the driver circuits of each switch. This is a very standard design for H-bridge converters.

Driver circuits

The main aims of this part of the design are the following:

- The MOSFETs must be switched in pairs of ten in parallel, simultaneously;
- The turn-on and turn-off times must be minimised, but in a way that will keep the voltage overshoot across the MOSFETs within limits;
- The conducting distance from the output of the driver to the gate of each MOSFET must be more or less equal to prevent too much difference in the inductance on the gates that will result in a difference in the switching times of the MOSFETs (see paragraph 22-6-3 in [G-10]).

The minimum turn-on and turn-off times of the MOSFETs, which are specified on the datasheets, are as follows:

$$t_{c(on)} = t_r = 90 \text{ ns}$$

$$t_{c(off)} = t_f = 71 \text{ ns.}$$

In this design, these times must be longer in order to minimise the voltage overshoot at turn-off. This dip compensator is digitally controlled with the PEC 31 DSP board and the voltage and current signals are sampled every 200 μs (see Chapter 5 on control). The minimum time in which a MOSFET can be turned on and turned off is therefore 200 μs . It will be therefore a safe practice if the turn-on and turn-off times of these MOSFETs are chosen as $t_{c(on)} = t_{c(off)} = 1.0 \mu\text{s}$.

The gate input capacitance of these MOSFETs is specified as $C_{iss} = C_{gd} + C_{gs} = 2.8 \text{ nF}$. From figures 22-11 and 22-14 in [G-10] it seems reasonable to assume that the turn-on/turn-off times are more or less equal to four times the time constant of the gate resistance (R_G) and C_{iss} . The gate resistance can therefore be designed according to the following formula:

$$4\tau = 4R_G C_{iss} = 1.0 \mu\text{s} \quad (4.7)$$

From this formula, the gate resistance is calculated as

$$R_G = 89.2 \Omega \approx 100 \Omega$$

Two gate drivers are used to drive two pairs of 5 MOSFETs in parallel, instead of connecting 10 gate resistances to the same gate driver, for each switch. This will give more equal distances from the outputs of the gate drivers to the gates of the MOSFETs. The block diagram of the driver circuit for each switch is included in Figure 4.7.

According to paragraph 22-6-2 in [G-10], the bias voltage of the MOSFETs must be high enough to minimise the 'on' resistance ($R_{DS(on)}$), but not too high for specifications stated in the datasheets. The bias voltage was chosen as $V_{GS} = 12 \text{ V}$. It will cause a peak current of $I_G = 12 \text{ V}/(100 \Omega/5) = 0.6 \text{ A}$. After considering all the possible digital and analogue options, the TPS 2813 driver chip of

Texas Instruments, with a 2 A peak output current rating, was chosen as the most cost-effective option. The maximum difference between the switching times of the two driver chips will be about 25 ns if the maximum differences of the rise and fall times and that of the propagation delay times are taken into account.

An analogue time delay (see Figure 4.8) is also included to implement dead time between the switches in each phase arm. The gate signal is fed from the gate signal multiplexer through an optic fibre. When V_{OPTIC} goes high, the capacitor C_D charge almost immediately through the diode D_D and this will cause the output of the driver to go low and turn the MOSFETs off. Otherwise, when V_{OPTIC} goes low, the capacitor C_D will discharge through R_D to implement a time delay of $2R_D C_D = 1 \mu\text{s}$ (theoretically), with $R_D = 270 \text{ k}\Omega$ and $C_D = 2.2 \text{ nF}$. It was found practically that this time delay is actually $4 \mu\text{s}$ and is caused by the high output impedance of the optic fibre receiver.

A photograph of a single inverter is shown in Figure 4.9.

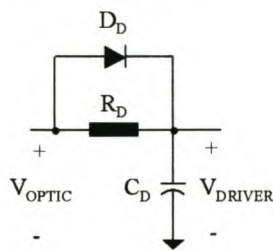


Figure 4.8: Analogue time delay circuit for each switch of the multilevel inverter.



Figure 4.9: Photograph of a single inverter with the isolated power supply and driver circuits on top.

4.3 Anti-parallel thyristors for protection

4.3.1 Selection

These components must be able to conduct the full load current, rated at $360 A_{RMS}$, continuously. It also has to be able to conduct fault currents at the load side of up to about twenty times the rated value for a short while. The breaking times of circuit breakers at these currents differ. The NS630N circuit breaker from Merlin Gerin can break this current in less than 60 ms (according to the datasheets).

In order to find the needed fault current capability, the i^2t value for the above conditions must be calculated. Manufacturers of thyristors give this value in the datasheets to assist in the selection of suitable fuses or breakers that have to protect these devices against damage due to short-circuits. For the above-mentioned conditions, a fault current of $7.2 kA_{RMS}$ for 60 ms will result in an i^2t value of $3.11 MA^2s$.

By taking this value into account, the SKT 1200 of Semikron was chosen (see photograph in Figure 4.10). It can conduct a current of $1200 A_{RMS}$ continuously and it has an i^2t value of $4.5 MA^2s$ at $T_{vj} = 25 ^\circ C$ (virtual junction temperature).



Figure 4.10: Photograph of two SKT 1200 thyristors.

4.3.2 Driver circuit

An existing isolated power supply and gate driver circuit for each of the two thyristors is used in this case. Figure 4.11 gives a block diagram illustration of this circuit. The isolated power supply looks much the same as the one that is used for the driver circuits of the MOSFETs. The only difference is that the pulse transformer has only one secondary winding and not three, as in the case of the MOSFET power supply.

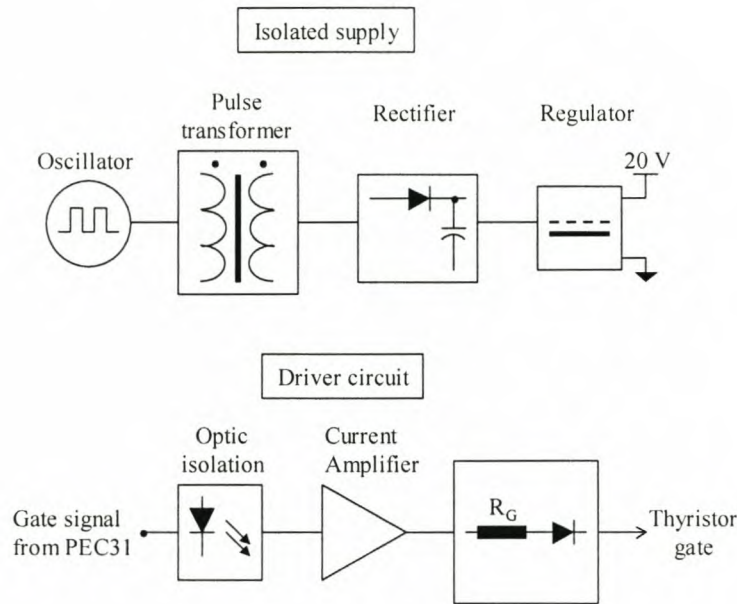


Figure 4.11: Block diagram of the isolated supply and driver circuits of the thyristors.

The gate signal of the thyristor is optically isolated by means of a LED and a photo diode on both ends of a black tube. The black tube shields the photo diode from any other light.

The gate resistance, R_G , of the thyristor is the fundamental part of the driver circuit. The value of this resistor is calculated from the values of the on-state gate voltage ($V_{GS(on)} = 1.65 \text{ V}$) and the minimum on-state gate current ($I_{GT} = 250 \text{ mA}$) of the thyristor. The value of the gate current for this design is chosen as 500 mA in order to decrease the switching time. R_G is calculated as follows:

$$R_G = \frac{V_{RG}}{I_G} = \frac{16.15}{0.5} = 32.3 \approx 33 \Omega$$

The power rating of this resistor is $P_{RG} = 33 \cdot (0.5)^2 = 8.25 \approx 10 \text{ W}$

4.4 Fault current detection

The purpose of the thyristors is to protect the multilevel converter from fault currents, as stated previously. An analogue detection circuit is used to detect fault currents on the line and its operation is illustrated in Figure 4.12. (The complete circuit diagram is also included in the datasheets.)

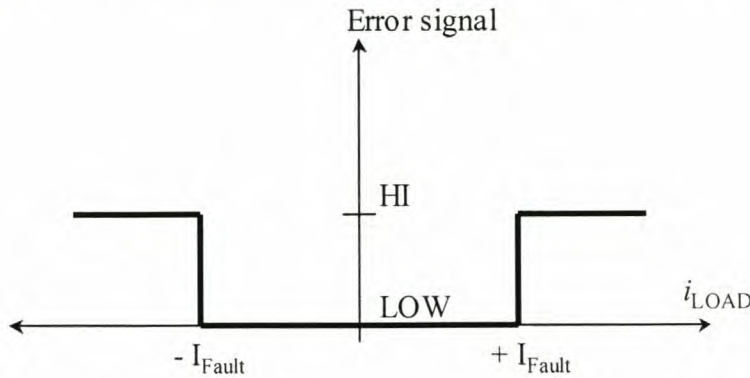


Figure 4.12: *Fault current detection principle.*

It basically consists of two comparators that compare the incoming current signal, from a LEM current sensor, with a positive ($+I_{Fault}$) and a negative ($-I_{Fault}$) threshold value. Both comparators' outputs are high under normal conditions. When the current rises above the positive or below the negative threshold, one of the comparators will give a low output to a NAND gate. The output of the NAND gate will go high and that will signal a fault condition to the DSP controller board (PEC 31) that controls the multilevel inverter. This signal will generate an interrupt that will initiate the necessary fault current protection procedure (explained in Chapter 5). The total propagation time delay from the instant when the fault current is detected up to the time when this fault signal reaches the PEC 31 controller board is less than $1\ \mu s$, according to the datasheets. The total time delay on the PEC 31 board, where both the DSP and FPGA are involved, cannot be accurately determined, but it seems that the thyristors will be fully switched on in less than $20\ \mu s$ after the signal has reached the PEC 31 board. The MOSFETs are switched off after a further delay of $100\ \mu s$. This delay is implemented to reduce the current through the MOSFETs when they are switched off.

The delays mentioned above raise the question if there is any possibility that the MOSFETs might get damaged. This possibility is determined by considering the maximum rate of change (derivative) for a $7.2\ kA_{RMS}$ sinusoidal current ($3.2\ A/\mu s$). The fault current threshold is set at about $600\ A$. If a fault current is detected at this threshold and a time delay of $21\ \mu s$ (from the above discussion) with the maximum rate of change is assumed, the current through the MOSFETs will rise to a value of $667\ A$ before the thyristors are fully switched on and start to conduct the current. As soon as the thyristors start to conduct the current (time delay of a few μs), the current through

the MOSFETs will start to decrease. The MOSFETs can then be switched off when a certain maximum value of the current is reached for a safe voltage overshoot.

4.5 Digital control of the multilevel converter for dip compensation

Two digital controller boards are used for the control of the multilevel converter for series dip compensation: a DSP controller board (PEC 31) and a gate signal multiplexer board.

4.5.1 DSP Controller board (PEC 31)

The DSP controller board (PEC 31) has already been developed at the University of Stellenbosch for control purposes of power electronic converters ([G-1],[G-12]). Figure 4.13 is a block diagram that illustrates the use of the PEC 31 controller in this compensator.

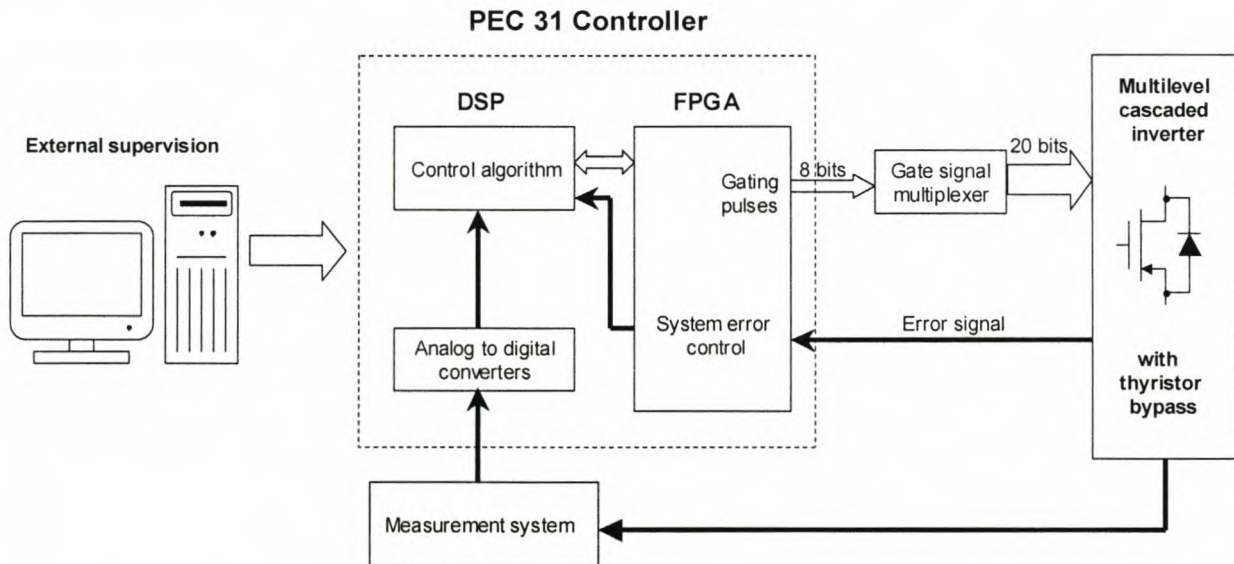


Figure 4.13: Implementation of the PEC 31 controller in the transformerless dip compensator.

The state of the dip compensator is determined by the measuring system. This measurement unit is calibrated to supply the controller with a representative voltage of the measured voltages (supply, load voltages) and the load current in a range that is easily digitised with available analogue to digital converters.

Once digital representations of the measured values are obtained, the DSP uses the control algorithm to calculate the actions needed to reach the desired next state of the dip compensator. These actions are then converted to gating signals. The FPGA has a facility to supply PWM gating signals to normal three-phase inverters. In this case a special facility (reconfigurable 8-bit output port) is used to supply the gating signals to the multilevel converter via the gate signal multiplexer by the FPGA. The FPGA is also used to process the fault current error signal from the multilevel converter in co-operation with the DSP control algorithm. This ensures a fast response time to protection circuitry and a high reliability. A personal computer is used as a supervisory controller to provide the necessary control algorithm and to display the system's information.

4.5.2 Gate signal multiplexer

The gate signal multiplexer was designed for this project to co-operate with the PEC 31 for the control of the multilevel converter. 20 gating signals are needed for the 5 individual H-bridge inverters in order to control the multilevel inverter for dip compensation. The gating signals are supplied from the PEC 31 controller board with an output port that is 8 bits wide. The 4 most significant bits are used to select the H-bridge inverter that must be switched and to latch the gate signals. The 4 least significant bits are used to define the gate signals for each of the 4 switches of the specific H-bridge inverter. An EPLD (Electric Programmable Logic Device) was programmed to multiplex these bits from the PEC 31 to form the gate signals to all the respective inverters. This EPLD is the EPM7064SLC44-10 from Altera. Figure 4.14 shows a diagram that explains the operation of multiplexing in the EPLD.

The 8-bit signal from the PEC 31 is divided into the gate signals ($SW[3..0]$), the 3 bits that define the inverter that must be switched ($CONV[2..0]$) and a latch signal ($LATCH$) that will latch the gate signals at the output of the multiplexer. The component $CONV_SEL$ is a 3-to-5 decoder that enables the flip-flop outputs that will pass the gate signals to the correct inverter. The *Gate signal filter* ($ANTI_SMOKE$) filters only the correct combinations of gate signals through to prevent short-circuits on the DC bus.

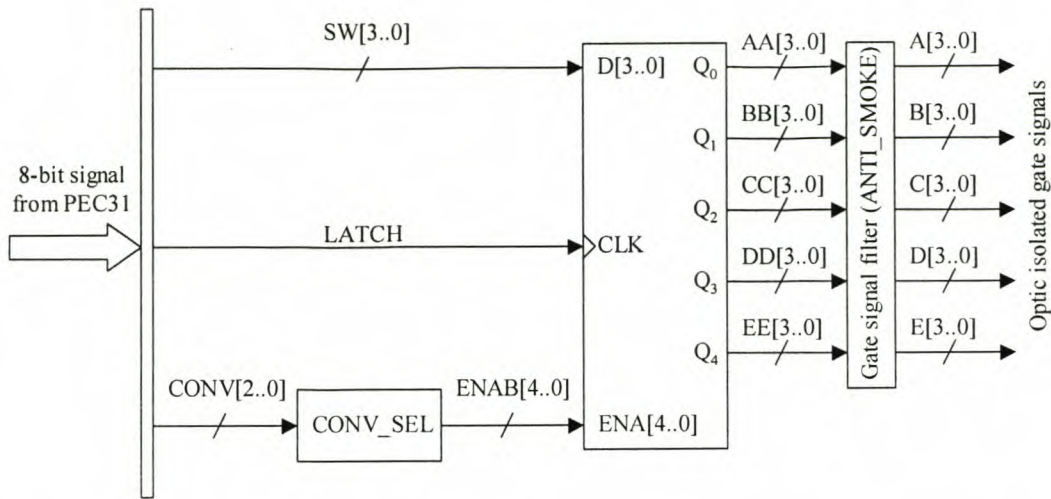


Figure 4.14: Schematic diagram of the programmed gate signal multiplexer in the EPLD.

Summary

This chapter discussed the hardware design of the series dip compensator (see photograph in Figure 4.15). It was designed for the most common dips up to a certain depth and duration. The advantage of this design is its modularity. It can be easily adapted for more severe dips by adding extra inverters for more severe dips (greater depth), because the average depth of dips varies from site to site.

Battery energy storage and MOSFETs as switching components proved to be the most cost-effective components for the specified ratings. The design of the DC bus was unique, because of the low voltage and high current ratings. DC bus capacitors were added to stabilise the DC bus voltage and also to compensate for reactive load currents. The anti-parallel thyristors were designed to conduct the line current continuously and to conduct fault currents of up to twenty times the rated current. A fault current detection circuit was therefore also designed.

Driver circuits were designed for the switching components and in the case of the MOSFETs the driver circuits must be able to switch ten MOSFETs in parallel.

The basic digital control was implemented with an established DSP control board. Finally, a gate signal multiplexer was designed to work together with this control board in order to implement the 20 gate signals needed for the multilevel inverter.



Figure 4.15: *Photograph of the whole single-phase dip compensator.*

5. Control of the multilevel converter for series dip compensation

5.1 Introduction

A lot of research papers are available on the control of multilevel converters. Two of these papers come close to describing this application. One of these papers [M-5] discusses series reactive current compensation. The other paper [M-4] is a rather incomplete theoretical paper with a few simulations on shunt voltage dip compensation with capacitive energy storage. Most of all the papers on multilevel inverters discuss control for steady-state, or close to steady-state conditions, while dips are transient phenomena that can change continually in depth. In spite of this, the control principles in all the papers on multilevel inverters ([M-1]-[M-13]) and also other inverters can still be used to derive a control algorithm for this application.

The uniqueness of this control algorithm is described by the following features:

- Fast response in small voltage steps that adapt quickly to changing circumstances. This can be achieved, because there are no delays caused by filter components, and fast switching components (MOSFETs) are used.
- The low switching frequency makes the control algorithm relatively simple and no balancing of capacitor voltages is needed.
- The transient nature of dips, though, complicates the sharing of battery energy storage and the sharing of power dissipation in the switching components. These sharing techniques are desirable in order to prevent certain components from decaying faster than others in this modular structure.
- Special fault current protection is needed for this series compensator.

This chapter starts with paragraph 5.2, giving an overview on the control principles that are used in this dip compensator. These principles are discussed in the rest of the chapter. Paragraph 5.3 discusses the first principle of dip detection. A few methods of dip detection are evaluated and reasons are given for the chosen method. In paragraph 5.4, the method of synchronisation is discussed in the same way. Paragraph 5.5 explains the simple method of voltage step control and gives reasons for this method. Paragraph 5.6 discusses the sharing method for the power dissipation in the switching components and the batteries. This method calls for a unique solution, because of

the transient nature of dips. The thyristor control methods are explained in paragraph 5.7. The complexities involved in the force commutation method and how they were overcome are discussed. This chapter also confirms most of the control methods in paragraph 5.8 with simulations and concludes with a summary.

5.2 Control principles

A diagram that describes all the principles, techniques and methods used to control this system for single-phase dip compensation is shown in Figure 5.1. The measured voltages and currents are sampled at 5 kHz (100 samples per cycle) by A/D converters on the PEC 31 control board.

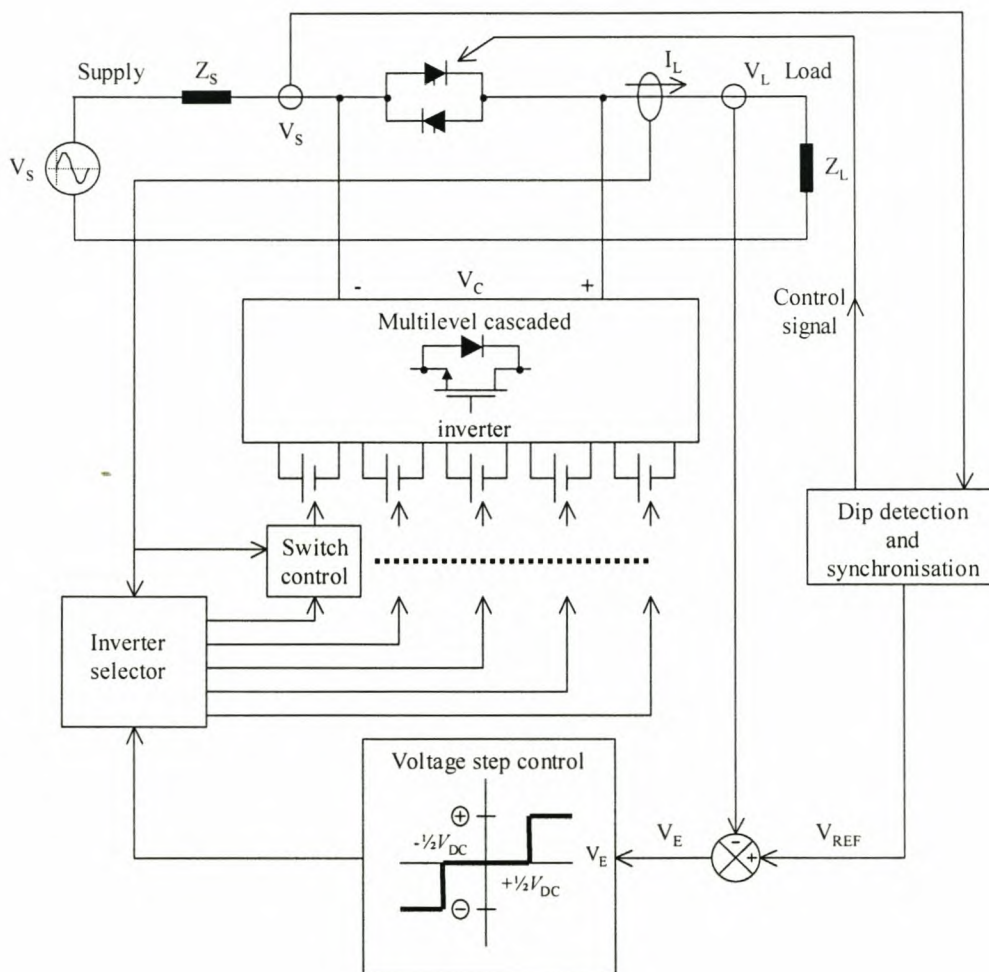


Figure 5.1: Block diagram of the control of the multilevel converter for dip compensation.

The multilevel inverter's principles of control for series dip compensation can be described as follows:

- a) *Normal conditions:* Under normal conditions, the thyristors conduct the full load current and all the MOSFETs in the multilevel inverter are switched off.
- b) *Initiation and termination of compensation:* When the line voltage drops below 90% of the nominal r.m.s. voltage, the thyristors are force commutated by the output of the multilevel inverter. The multilevel inverter then starts to inject a staircase voltage waveform in series with the line. The compensation is terminated when the line voltage rises above 90% of the nominal r.m.s. value or if the energy storage is depleted. The output of the multilevel inverter is first switched to the zero output state, and then the thyristors are switched on. The multilevel inverter is switched off after a sufficient turn-on delay for the thyristors.
- c) *Injection of the staircase sine waveform:* The generation of this waveform is based on the single-pulse technique, method B [M-5]. This method can be explained by Figure 5.2 [M-5]. It shows that the voltage pulses contributed by each individual inverter are terminated in the same order that they are initiated. This method is one way to level the duration of discharge for each DC bus, but it will not make it equal. According to [M-5], the maximum deviation of the discharge values for five inverter units is about 10% if the injected voltage is sinusoidal.

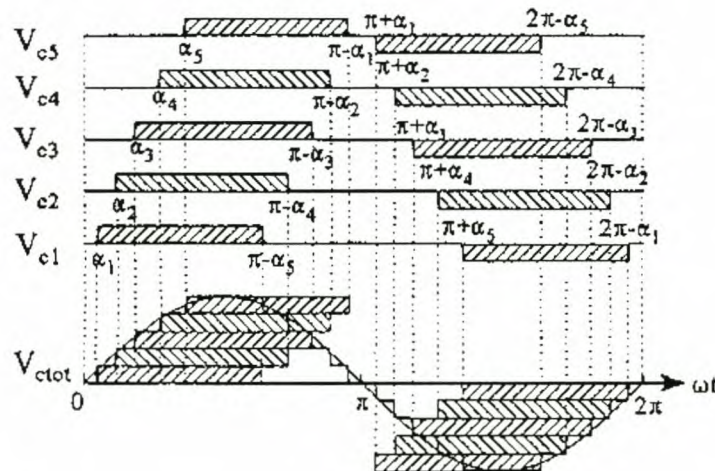


Figure 5.2: Single-pulse technique for the generation of the staircase sine waveform.

- d) *Sharing of the power dissipation:* The necessity of this feature was already stated in the introduction. Sharing of the power dissipation in both the switches and the batteries can be achieved by continuously changing the switching order of the individual inverter units [M-13] and also by utilising redundant switching states [M-1].

- e) *Protection:* When a fault occurs on the load side of the compensator during a dip, the multilevel inverter must cease its operation as soon as possible and the thyristors must take over the fault current simultaneously until the necessary circuit breaker is opened.

The strategies for all of these control principles will now be discussed.

5.3 Dip detection

It was stated in the previous paragraph that this compensator must initiate compensation as soon as the line voltage drops below 90% of the rated r.m.s. value. The required response for a dip will vary with different loads. The most sensitive loads, like the one discussed in Figure 2.7, will trip after only half a cycle. It is therefore a safe practice to limit the response time to less than a $\frac{1}{4}$ cycle or about 4 ms* after the voltage has dropped below 90% of the rated value. The dip detection technique should also be insensitive to distortion in the line voltage. A few dip detection techniques were evaluated and compared.

a) *Measuring the r.m.s. value*

In this technique the samples of the supply voltage, in a moving window over the past cycle, are used to calculate the r.m.s. value in a discrete manner with the following formula:

$$V_{RMS} = \sqrt{\frac{1}{T} \int_{t_0-T}^{t_0} v^2(t) dt} \quad (5.1)$$

In this formula v represents the supply voltage, t_0 represents the time instant at which this value is calculated and T is the period of one cycle. According to [C-17], this value is only accurate for steady-state circumstances and it takes a full cycle to determine the actual depth of the dip, because it is calculating an average value of the past cycle. The response of this method is therefore too slow.

b) *Hysteresis technique*

This technique uses two reference signals in phase with the phase voltage. These signals have positive and negative DC offsets of about 10% of the amplitude. The phase voltage is compared

* The 4 ms response time was suggested by Ian Smit from Eskom.

with these reference signals. As soon as it drops below the lower reference signal in the positive half cycle or rises above the upper reference signal in the negative half cycle, the dip will be detected. This technique is illustrated in Figure 5.3.

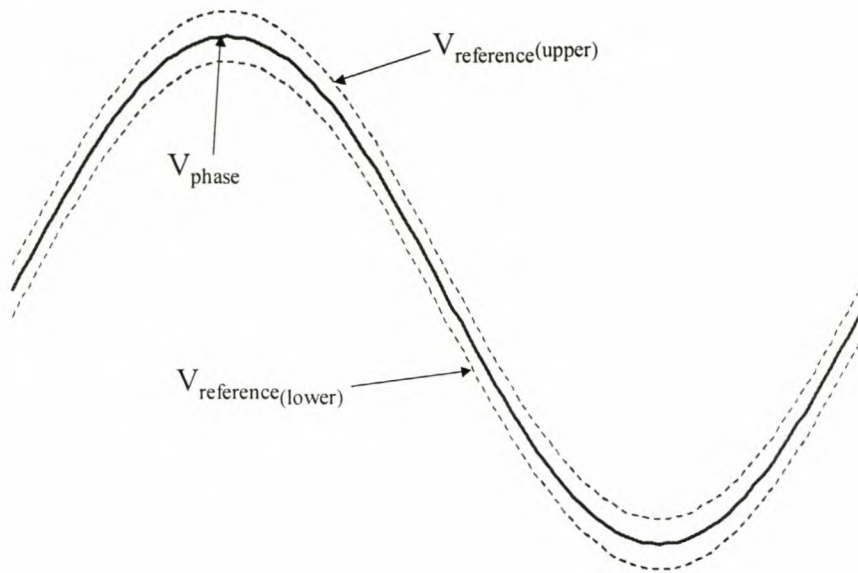


Figure 5.3: *Dip detection with the hysteresis technique.*

The advantage of this technique is that you get an immediate response. The problem is that this type of detection can be very noisy, because it will also detect signal distortion and this will result in false responses. In order to avoid signal distortion, the voltage signal may be filtered before it is compared with the two references, but this will result in a time delay and a phase shift of the measured signal.

c) Calculating the DFT

The Discrete Fourier Transform (DFT) is normally used to calculate the amplitudes and phase angles of a discrete fundamental frequency component, and also at discrete multiples of this frequency, for a sampled waveform in a certain time window [C-14]. The formula for a DFT is defined as follows:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N} \quad k = 0, 1, \dots, N-1 \quad (5.2)$$

In this formula $x(n)$ defines the sampled waveform with N samples. $X(k)$ represents the calculated discrete frequency components. If the fundamental frequency component is set equal to the line frequency, the amplitude of the supply voltage signal can be calculated from the following simplified formula, derived from (5.2):

$$X(1) = \sum_{n=0}^{N-1} (x(n)) (\cos(2\pi n/N) - j \sin(2\pi n/N)) \quad (5.3)$$

The amplitude of the supply signal can then be calculated from the N sampled values in a moving window over the previous cycle. Precalculated values of the sine and cosine waveforms can be used to accomplish this.

A simulation of the dip detection with this method is shown in Figure 5.4. A dip with a depth of 30%, a phase shift of 30 degrees and a duration of 6 cycles on a single phase line with a 50 Hz phase voltage of 230V_{RMS} was simulated. This simulation shows that this method also has a slow response. It also takes a full cycle (20 ms) to determine the actual depth of the dip as in the case of the r.m.s. value.

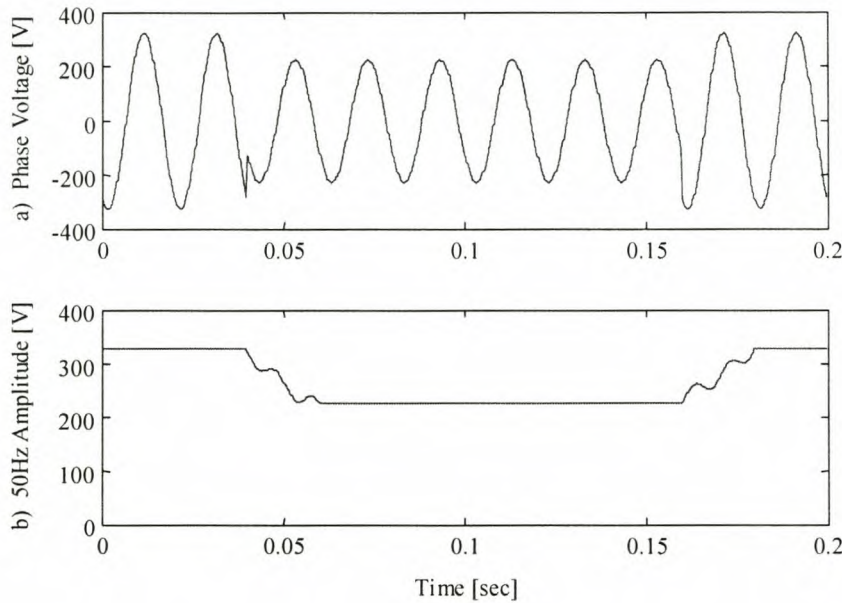


Figure 5.4: Simulation of dip detection with the DFT technique.

d) Calculating the $\frac{1}{4}$ cycle relationship [G-16]

Refer to Figure 5.5 for an explanation of this dip detection method. It is assumed that the supply voltage is sinusoidal with amplitude A . The dip detection is done by defining the instantaneous value of the phase voltage at time $t_0 + T/4$ as $A \cos(\omega t_0 + \Phi)$, and at time t_0 as $A \sin(\omega t_0 + \Phi)$. The amplitude of the supply voltage can then be determined by making use of these two values and the identity in (5.4).

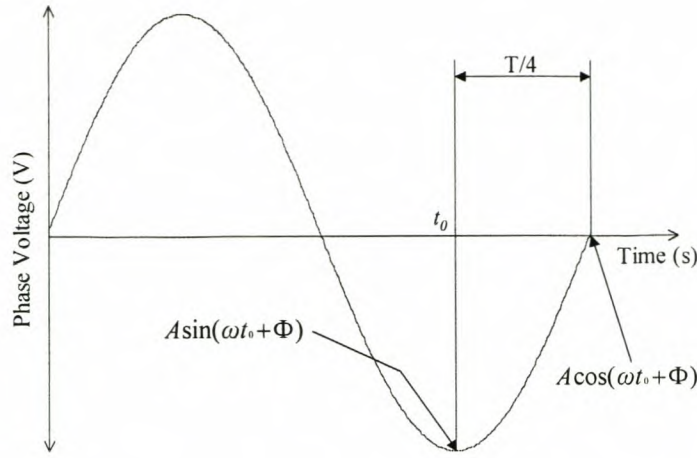


Figure 5.5: Principle of dip detection with the $\frac{1}{4}$ cycle relationship.

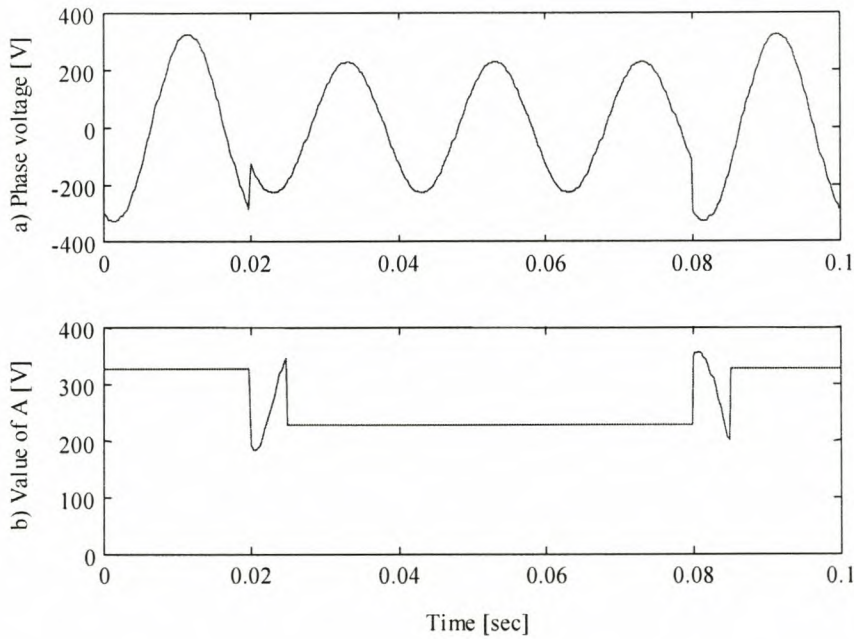


Figure 5.6: Simulation of dip detection with the $\frac{1}{4}$ cycle relationship.

$$A = \sqrt{(A \sin(\omega t_0 + \phi))^2 + (A \cos(\omega t_0 + \phi))^2} \quad (5.4)$$

This method gives an immediate response in case of a dip. A simulation of this method is shown in Figure 5.6 for a 230 V_{RMS}, 50 Hz voltage with a dip depth of 30% starting at $t = 0.02$ s and ending at $t = 0.08$ s. The simulation in Figure 5.6b shows an immediate drop in the calculated amplitude when the dip occurs, but a transient with a $\frac{1}{4}$ cycle duration follows each change in amplitude. This method is also sensitive to glitches and harmonics on the supply voltage. Therefore, instead of just calculating A , the average value of A in a moving window, over the previous quarter cycle, is

calculated to detect a dip. A simulation of the improved method is shown in Figure 5.7 for the same simulated dip in Figure 5.6a. This simulation shows that a dip with a 30% depth can be detected within 1 ms after it started, if the sag detection level is set for 90% of the nominal amplitude. The actual depth of the dip is determined after only half a cycle.

The previous three methods either have a too slow response or they are too sensitive to noise. This method has a relatively fast response and is not too sensitive to noise and is therefore accepted as a suitable method for single-phase dip detection. Three-phase control methods ([C-4],[C-6],[C-10]), which use the phase and amplitude relationships, exist and they will give a faster, cleaner response to dips. An example of these methods is the dq0 transformations, used in AC motor speed control.

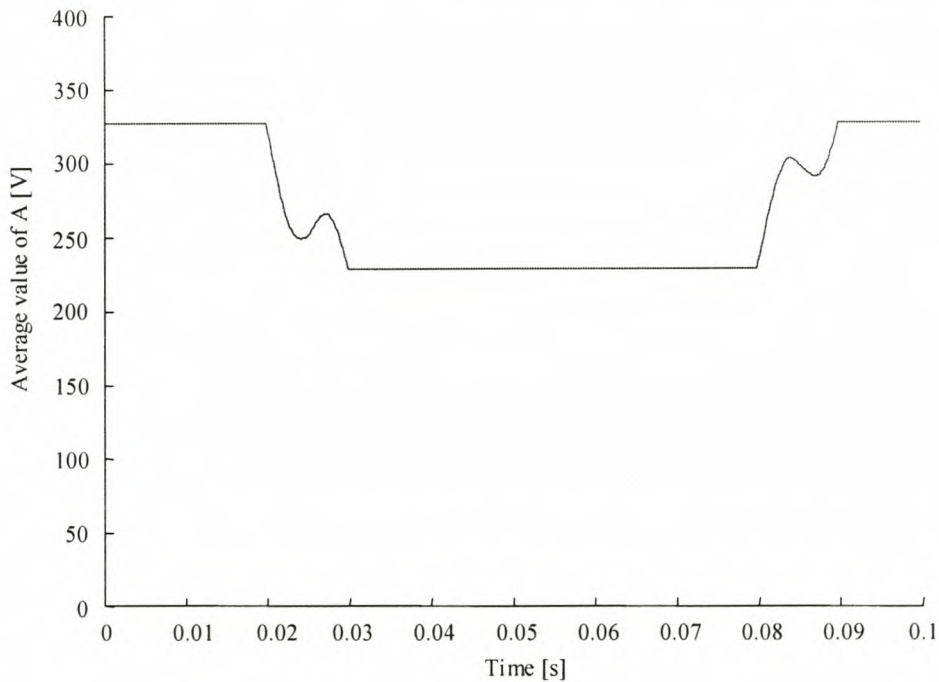


Figure 5.7: *Simulation of dip detection by taking the average value of 'A'.*

5.4 Synchronisation

This is also a very important part of the control that needs a lot of attention. The method of synchronisation should be accurate and it must not be too sensitive to signal distortion on a power line. An important fact is that this method is used for single-phase load compensation. This implies that the reference phase angle doesn't have to be synchronised to the original phase voltage during the phase jumps (discussed in paragraph 2.3) in a dip. It is still preferable that the reference phase gradually adapts to the phase jumps in a dip in order to protect phase-sensitive single-phase loads. The considered synchronisation methods will now be discussed.

a) Zero-crossing technique

This technique has been widely used in the control of three-phase thyristor bridges or other thyristor-based converters. A well-known example is 6-pulse, line-commutated ac to dc converters. The principle of this technique is to detect the instant when the expected sinusoidal supply voltage crosses zero volts and synchronises the control accordingly. Voltage distortion phenomena like spikes and notches may cause multiple zero crossings at the crossover point. These phenomena will make this method very inaccurate as is illustrated in Figure 5.8 (a)-(c) [C-18] for voltage notches. Figure 5.8 (a) and (b) shows the delay that may occur in the reference signal due to the notches in the waveform. An even worse delay may occur when two positive transitions are detected shortly after each other, as illustrated in Figure 5.8 (c).

Several solutions exist [C-18] to overcome this problem, related to distortion:

- Voltage sensing at the primary side of the converter transformer;
- Using a lowpass filter;
- Using a bandpass filter;
- Predictive linearisation;
- Open-loop voltage-drop compensation.

The following problems and limitations are encountered with these solutions:

- The zero-crossing signal instant is load-current and firing-angle dependent;
- The zero-crossing signal is sensitive to load transformer impedance and frequency variations;
- The zero-crossing method is valid for a restricted range of commutation overlap angles;
- The zero-crossing signal cannot be ascertained in real time;
- Specialized instrumentation is required.

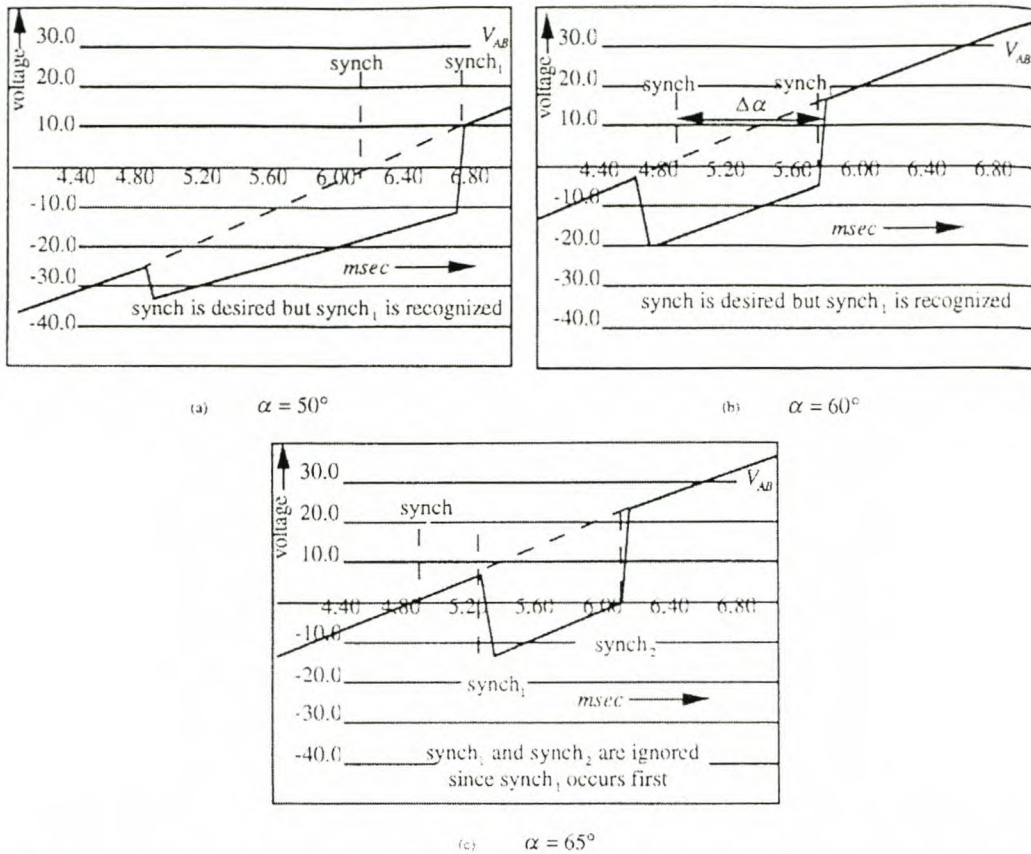


Figure 5.8: Three cases of false crossover detection caused by voltage notches.

Reference [C-18] discusses an advanced method, referred to as adaptive online waveform reconstruction, which is based on the estimation of the converter source commutation inductance. In essence this method indirectly obtains a zero crossing of the synchronisation signal from a waveform inferred online from the converter line-to-line voltage and two of the line currents. In this method a delay of several cycles is required in order to estimate the correct value of the source inductance.

b) Phase locked loop (PLL)

The basic phase-locked loop consists of a signal multiplier (i.e. a balanced modulator), a low-pass filter and a voltage-controlled oscillator (VCO), as shown in Figure 5.9. Operation of the phase-locked loop when the VCO frequency is near the incoming frequency is as follows. The incoming sinusoidal signal, $\cos \omega_{ct}$, is multiplied by the output of the VCO. The low-frequency component of the output of the multiplier is a voltage whose magnitude and sign are proportional to the phase difference, for small differences, between the incoming sinusoid and the VCO. This voltage is used to control the VCO and the loop attempts to keep the phase difference small (ideally, zero) between

the VCO signal (the synchronising signal in this case) and the incoming signal (supply signal). The objective of synchronisation between the two signals has thus been accomplished.

A lot of research papers ([C-1],[C-3],[C-4],[C-6],[C-17]) that use variations on this technique are available. This method works well for steady-state power-quality problems, but it will create a problem for transient compensation. The reason is that this method takes a few cycles [C-1] to synchronise to the supply and this creates a problem in the case of the sudden phase shift introduced at the beginning and end of a voltage dip. An advanced PLL method [C-17], called the *Missing Voltage Technique*, retains synchronisation with the original phase voltages when phase jumps occur during a dip. This method is suitable for three-phase synchronisation, but it will not be considered due to the reasons stated at the beginning of this paragraph.

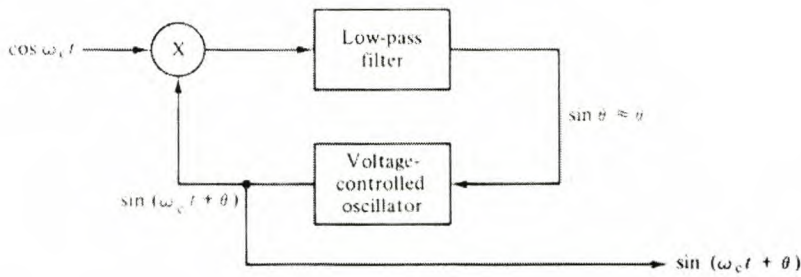


Figure 5.9: Block diagram of a basic phase locked loop (PLL).

c) Using the $\frac{1}{4}$ cycle relationship

In the same way as described in paragraph 5.3, a synchronised reference signal can be determined for single-phase dip compensation from this technique. From Figure 5.5 and equation (5.4) a unity, synchronising signal can be easily obtained. This is implemented by dividing the instantaneous value, $A\cos(\omega t_0 + \Phi)$, by the value obtained from equation (5.4). The reference signal was simulated for the same conditions as in Figure 5.6 (*depth* = 30%, *phase shift* = 30° , *duration* = 3 cycles, starting at 0.02s, and *phase voltage* = $230V_{RMS}$). This simulation is shown in Figure 5.10. This simulation shows that the phase jumps at the beginning and the end of the dip cause jumps in the reference signal that can cause problems in dip compensation for phase-sensitive loads. This synchronising technique is also very sensitive to distortion.

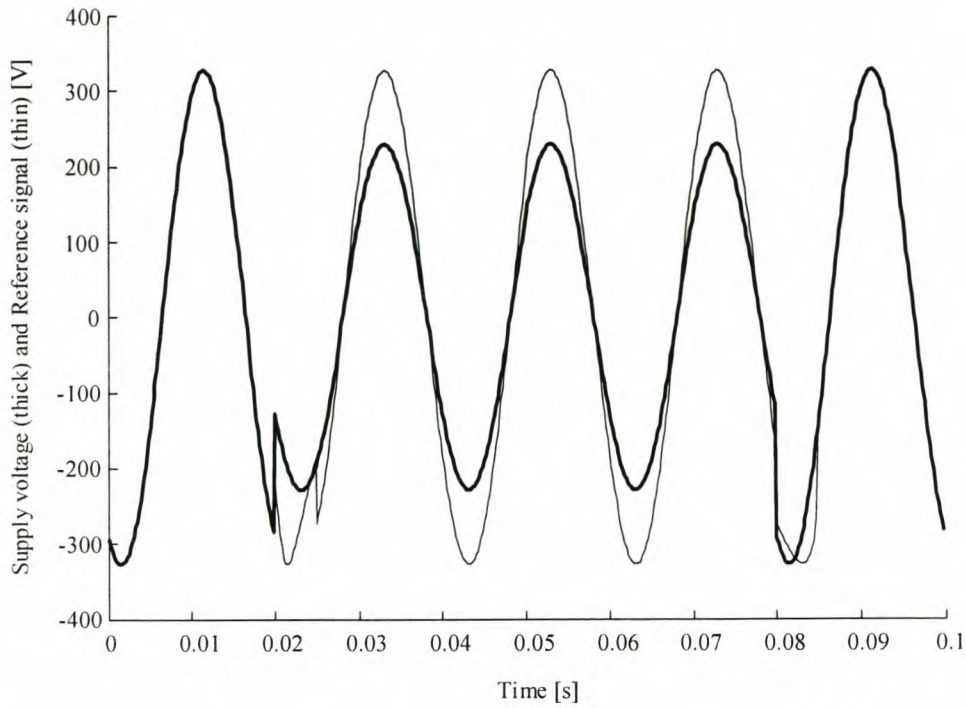


Figure 5.10: Phase voltage and reference signal during a dip generated through the $\frac{1}{4}$ cycle relationship.

d) Correlation technique

Synchronisation through this technique is implemented with the samples in a moving window, i.e. the previous cycle's sampled values. These values are compared to precalculated values of a sine waveform by phase shifting the samples until a best fit is found. This method is implemented by the following formula [C-14]:

$$r_{ps}(l) = \sum_{n=0}^{N-1} p(l)s(n-l) \quad l = 0, \pm 1, \pm 2, \dots, \pm(N-1) \quad (5.5)$$

where p represents the sampled phase voltage and s the saved sinusoidal signal.

A simulation of the reference signal, generated by this method, is shown in Figure 5.11. This was done for a dip with a depth of 30%, a duration of 4 cycles (0.04 - 0.12s) and a 30° phase shift at a phase voltage of $230V_{\text{RMS}}$.

This simulation shows that the reference signal has a more gradual transition at the phase jumps at the beginning and end of the dip. It takes one cycle to adapt to the phase jumps. This delay is acceptable. The concept of taking a whole cycle's values into account also makes this method less susceptible to distortion. One drawback of this method is that it involves a lot of calculations (19 900 calculations at every sampling instant for $N = 100$ samples per cycle).

e) DFT technique

This technique was explained in paragraph 5.3 by which the phase of the supply signal can be derived by equation (5.3). The same dip with the same conditions as in Figure 5.11, is simulated in Figure 5.12 for the DFT technique.

In this simulation it is clear that the DFT technique gives almost exactly the same response as the correlation technique. This method is also less susceptible to distortion for the same reason as in the correlation technique's case. The advantage of this technique is that the number of calculations is far fewer (100 times less in the case of $N = 100$ samples per cycle) than for the correlation technique.

If all the synchronisation techniques are compared, it again shows that the techniques with the fastest response (zero crossing and $\frac{1}{4}$ cycle) are more susceptible to noise, while the rest of the techniques have a slower response but are less susceptible to noise. Of the latter, the DFT and correlation techniques have a faster response than the phase locked loop. The DFT technique has fewer calculations and this technique is therefore chosen as a suitable method for synchronisation in single-phase dip compensation.

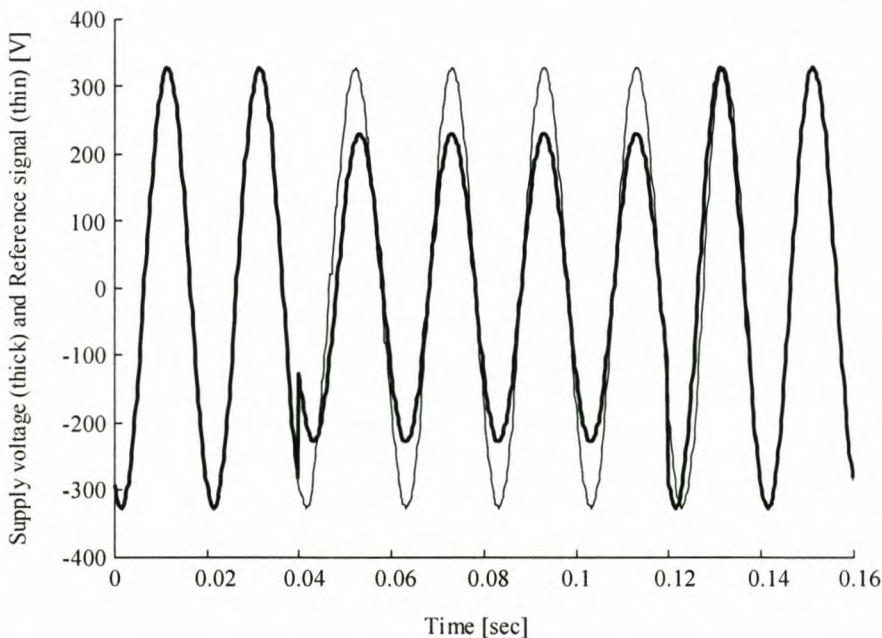


Figure 5.11: Phase voltage and reference signal generated by the correlation method during a dip.

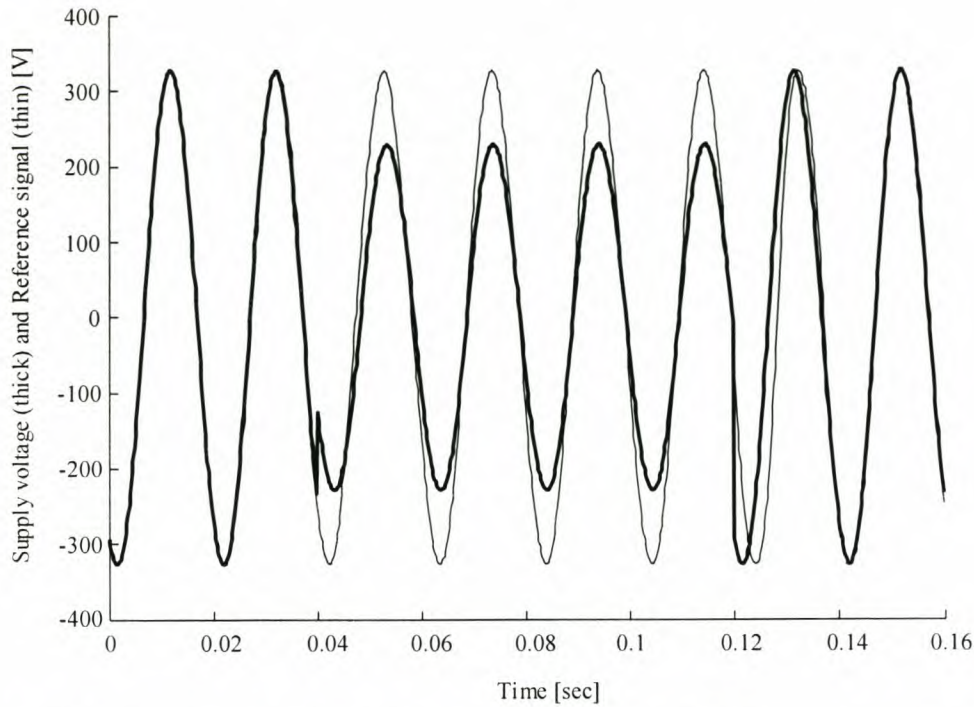


Figure 5.12: Phase voltage and reference signal generated by the DFT technique during a dip.

5.5 Voltage step control

The amplitude of this waveform is established through the number of voltage steps in each cycle by using a simple voltage step control method. This method enables the compensator to continue compensation when the depth of the dip increases beyond the predefined 30%. In the research papers on this topic ([M-5],[M-6],[M-10],[M-12],[M-13]) all the voltage steps are used in each cycle. The amplitude is controlled by using tables with precalculated switching angles ($\alpha_1, \alpha_2, \dots, \alpha_N$) for each modulation index in a way that will minimise the harmonic content. The depth of dips in practice can vary in one cycle and the latter method is therefore not practical.

Figure 5.13 explains the voltage step control method. When a dip is detected, the deviation in the absolute error voltage ($|V_E|$) must be more than half of the step voltage (more or less $\frac{1}{2} V_{DC}$) to add or subtract another voltage step at the output of the converter. This method gives rise to a simple way to make the area of the voltage step, under the error voltage waveform (V_E), more or less equal to the area of the voltage step, above V_E . If these areas are equal certain harmonics can be eliminated [M-5]. The simple technique suggested here is easy to implement and provides close to optimal results. The example in paragraph 3.2.3 showed a THD of 6.28% for the sinusoidal staircase waveform generated with this method in Figure 3.3.

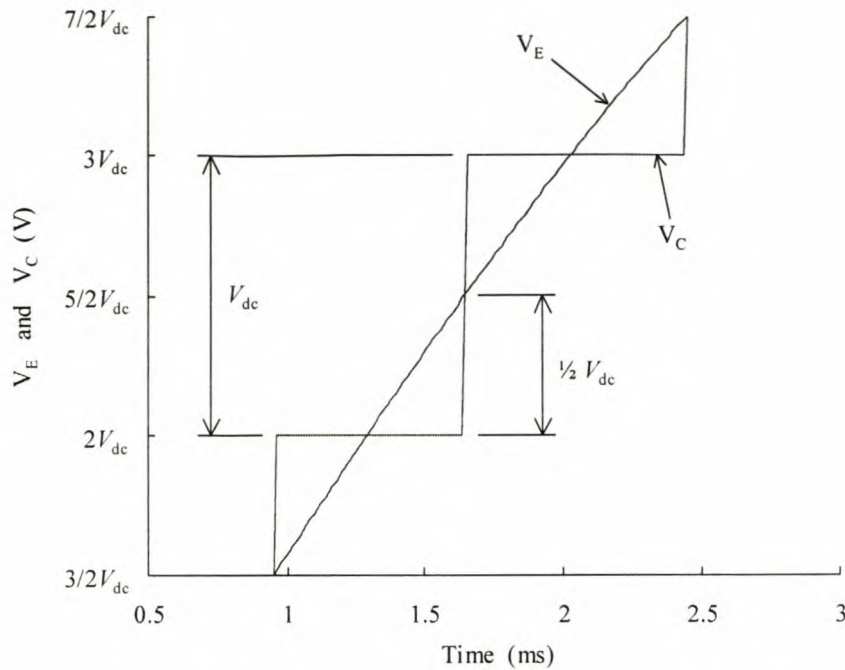


Figure 5.13: *Illustration of the voltage step control method.*

5.6 New method power dissipation sharing

The multilevel structure of this inverter requires effective sharing of the power dissipation in the MOSFETs and the batteries on the DC buses. Although the batteries used in this application have quite a large capacity, it will be an advantage if their discharge is roughly shared. These features are important, because they will prevent certain batteries and MOSFETs from decaying faster than the others.

The research papers on multilevel inverters showed a way of sharing the discharge of and power dissipation in the separate DC buses [M-13]. By rotating the order in which the voltage steps are added and subtracted for each half cycle, sharing of the discharge can be achieved for relative steady-state conditions. This rotating order can be stored in a look-up table with precalculated switching angles ($\theta_1, \theta_2, \dots, \theta_5$ in Figure 3.3) for each modulation index, M_i , in a way that will minimise the harmonic content. References [M-1] and [C-9] discuss a method of sharing the power dissipation in the switching components in multilevel inverters. This is implemented by using the redundant zero-output states of each inverter as illustrated in Figure 5.14. The switching of the inverters can be implemented in a specific order from a look-up table, in the same way as above, to achieve sharing of power dissipation under relative steady-state conditions.

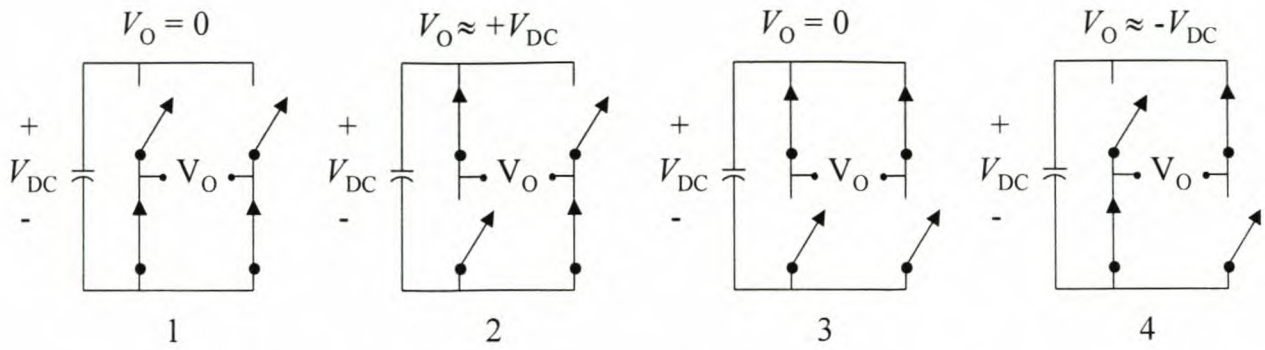


Figure 5.14: Four possible switching states for each inverter.

It was stated previously that the depth of dips might vary in one cycle, because of the transient nature of dips. The methods as described above will therefore not be effective. A new method, which implements the sharing of the power dissipation in the DC buses and also the sharing of power dissipation in the switching components simultaneously, had to be developed. This method is based on the above methods and will now be explained.

An observer that estimates the power dissipation in each of the four switching states, illustrated in Figure 5.14 for each inverter, is implemented. This is done by integrating the square of the current for each switching state of each inverter, because each switch can be approximated as a resistance in the on-state and the internal impedance of each battery can also be approximated as a resistance. The way these values are used in this method is explained through Figure 5.15. In the positive half cycle these values of state 2 of all the inverters are compared to determine which inverter must add or subtract a voltage step (Figure 5.15a). The same method is followed for these values of state 4 in the negative half cycle (Figure 5.15b). At the end of each half cycle the integrated values of state 1 and 3 are compared for each inverter to determine the most economic zero switching state, i.e. the state with the least power dissipation at that stage, for each inverter (Figure 5.15c).

At the end of each dip, these values are reset to zero to prevent overflowing values in the DSP.

This method implements the sharing of the power dissipation in the switches and the batteries, simultaneously, under transient conditions. The discharge of the batteries is also roughly shared. The sharing of the power dissipation is verified in the simulations at the end of this chapter.

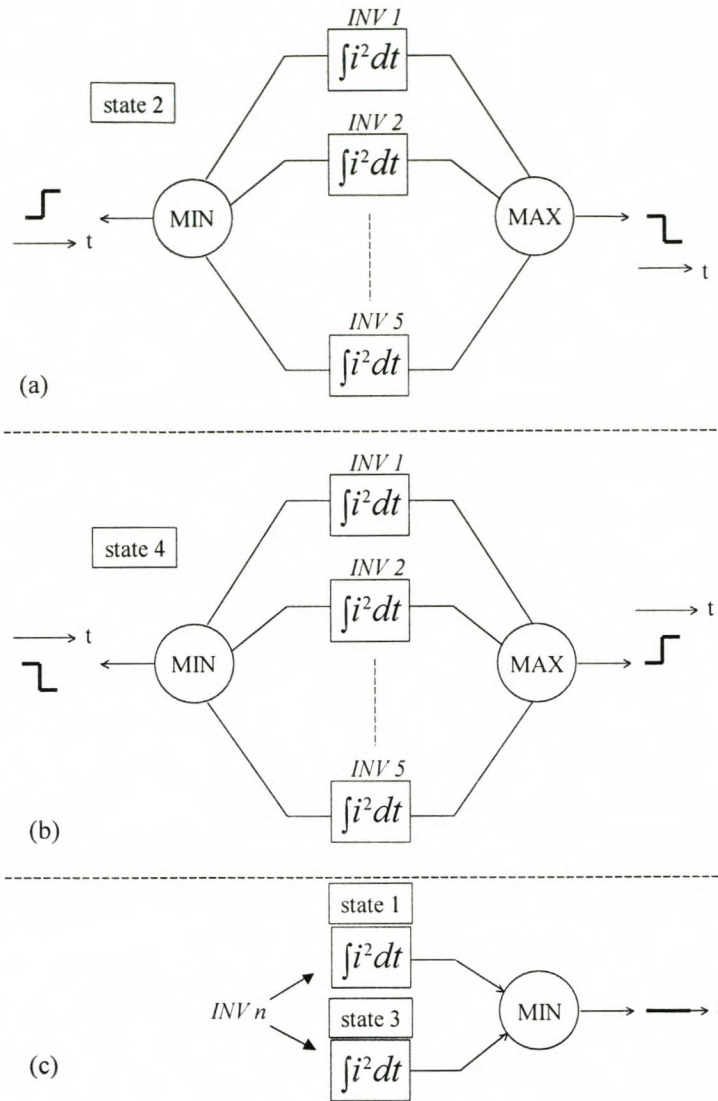


Figure 5.15: Block diagram representation of the new method for power dissipation sharing.

5.7 Thyristor control

It was previously stated that the anti-parallel thyristors, in parallel with the multilevel inverter, serve two purposes: conduction of the line current under normal conditions and protection of the multilevel inverter from fault currents. The control of the thyristors, for the transitions involved in these applications, will now be discussed.

5.7.1 Initiation and termination of compensation

When a dip is detected, the thyristors must be switched off as soon as possible to start compensation by means of the injection of the staircase sine waveform with the multilevel inverter. This implies that the thyristors first have to be force commutated before a voltage can be injected. The multilevel converter performs this force commutation with a voltage at its output across the thyristors. When applying this technique the bypass switch can be opened in approximately one millisecond. This is in contrast with the half-cycle commutation times usually associated with thyristor-based switches. Two conditions need to be taken into consideration to make this method effective. Firstly, the sign of the injected voltage has to be the same as the sign of the load current in order to commutate the thyristor bypass. This implies that if the dip is detected during period t_p . (Figure 5.16), the inverter effectively has to generate a very brief dip to commutate the bypass before actively compensating the dip on the supply voltage. The case where the sign of the load current changes during thyristor commutation also requires special attention and is part of the rest of this discussion.

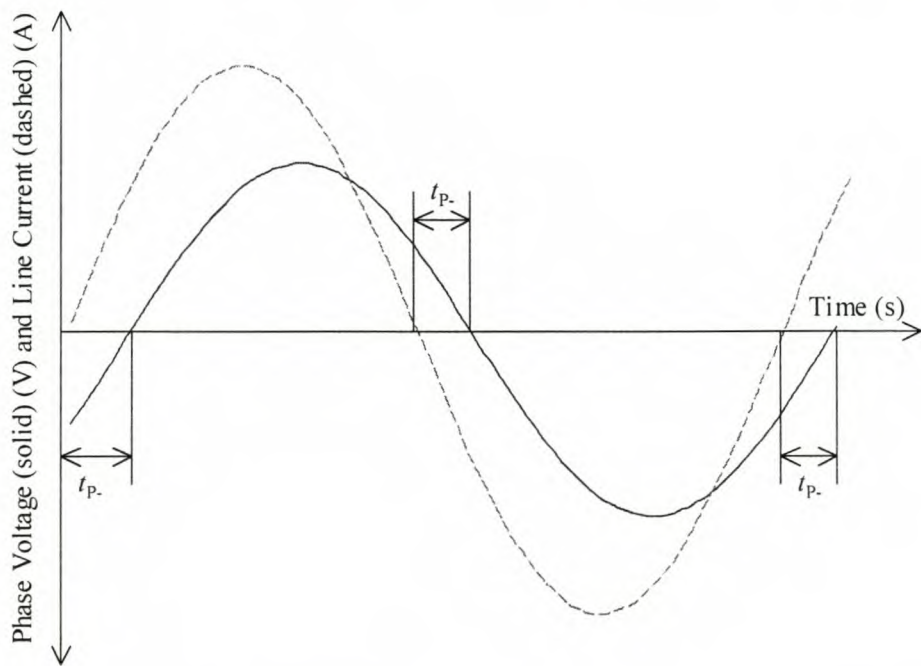


Figure 5.16: Illustration of the critical time period for the force commutation of the thyristors.

A not so obvious condition that requires attention is the time period t_{rr} when the reverse recovery current flows during turn-off of the thyristors. Figure 5.17 illustrates this problem for the positive half cycle of the load current (I_{LOAD}), where I_{RRC} represents the direction of the temporary reverse recovery current and V_{INJ} , the voltage injected by the multilevel inverter. For this time period the

output of the multilevel converter effectively ‘sees’ a short-circuit that may create an over-current condition. This can activate the over-current protection of the converter. To overcome this problem, the following new method, illustrated in Figure 5.18, is used to accomplish force commutation: when a dip is detected, the individual inverters are all switched in their zero state in order to provide a parallel path for the current flow. A very short pulse (5 μ s in duration) from one of the individual inverters is applied across the thyristors, according to the current polarity. This will result in a decrease in the thyristor current and a resulting increase in the current through the inverters. After a certain time delay (100 μ s), another longer pulse (50 μ s) is applied across the thyristors, again according to the current polarity, which brings the current flow through the thyristors to an abrupt end (before the end of the 50 μ s pulse). By detecting the current polarity before each pulse, the transition of the sign of the load current is taken into consideration.

When the thyristors are force commutated with these pulses, the multilevel inverter starts to inject a voltage after another time delay $t_q = 250 \mu$ s. This value is specified in the datasheets of the thyristors and represents the time interval from the instant when the thyristor current has decreased to zero to the earliest instant when the thyristor is capable of supporting a steeply rising reapplied off-state voltage without breaking over.

This method is verified in the simulations and the practical results.

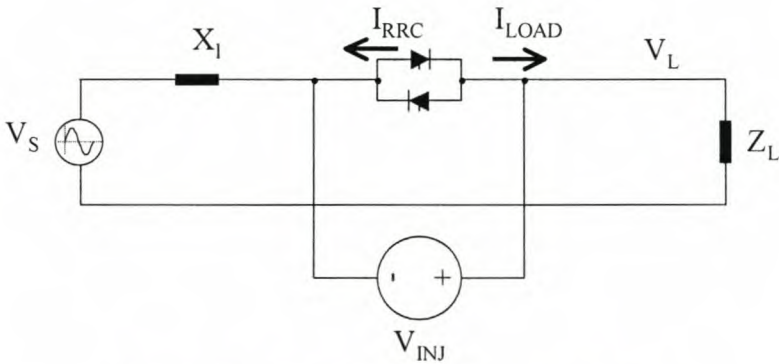


Figure 5.17: Force commutation problem.

When compensation is terminated, the individual inverters are again switched in their zero state before the gates of the thyristors are switched on in order to prevent a short-circuit condition. After a sufficient delay (200 μ s), for the thyristors to turn off, all the inverters are switched off, i.e. all the MOSFETs are switched off.

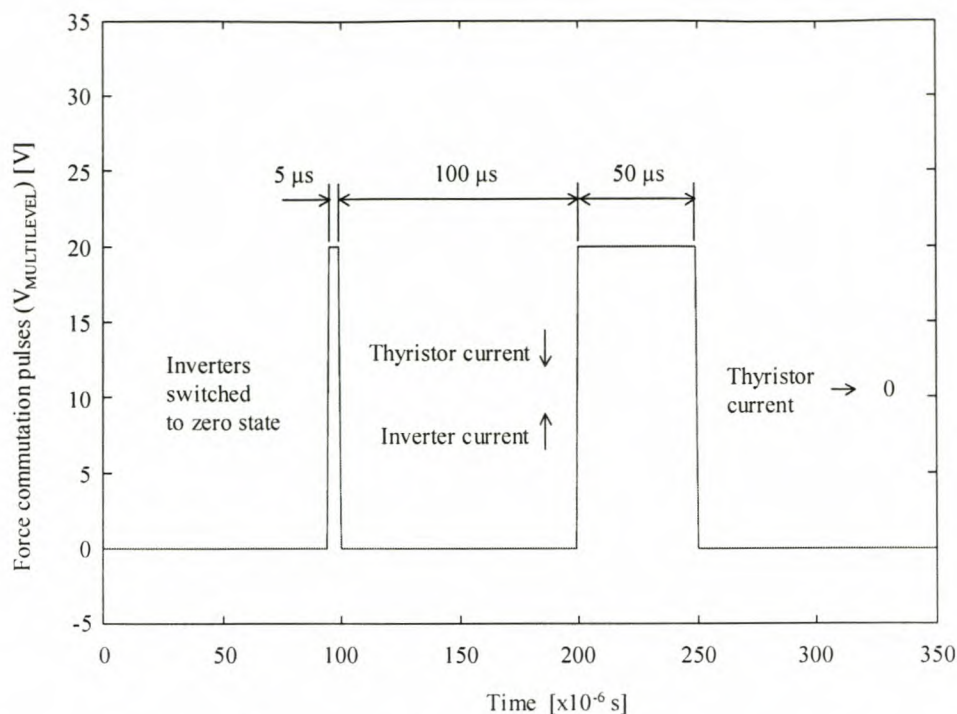


Figure 5.18: *Illustration of the method for force commutation.*

5.7.2 Fault current protection

Although MOSFETs can tolerate over current for a short duration, this part of the control still needs to respond quite fast. The fault current is detected according to the method in paragraph 4.4. If a fault current is detected during compensation, the compensation is terminated in the same way as it is terminated under normal conditions. The only difference is that the delay, intended for the turn-on of the thyristors, can be extended to ensure a sufficient increase in the thyristor current and a resulting decrease in the inverter current before the MOSFETs are switched off.

5.8 Simulations

A simulation study was done with the Simplorer simulation package to verify the control techniques for dip compensation with a multilevel inverter developed in this chapter. Simulations of dip compensation at dips with different depths and at different loads are discussed first. The new techniques of power dissipation sharing and the force commutation method, together with a simulated staircase sine waveform, are also verified through the simulations.

Table 5.1: Basic parameters of the simulations.

| Parameter | Value |
|---------------------------------------|----------------------|
| Supply voltage (V_s) | 230 V _{RMS} |
| Load current (I_L) | 360 A _{RMS} |
| Line frequency | 50 Hz |
| Separate DC bus voltages (V_{DC}) | 24 V |
| Dip duration | 7 cycles (140 ms) |
| Initiation time instant | 42 ms |
| Termination time instant | 182 ms |

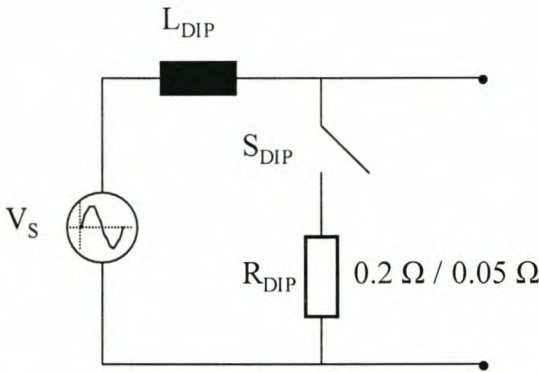


Figure 5.19: Generation of simulated dip.

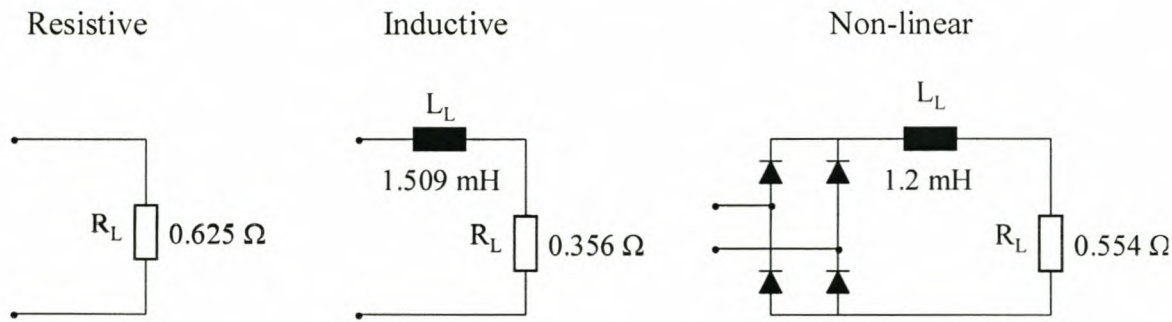


Figure 5.20: Different loads that were tested for dip compensation in the simulations.

The basic simulation set-up was done according to Figure 5.1. Table 5.1 gives the basic parameters for all the simulations. The dip initiation time only differs for the simulations on the various conditions for force commutation with an inductive load (Figure 5.35 - Figure 5.38). Figure 5.19 illustrates the method of dip generation in the simulation. When the switch, S_{DIP} , is closed, a large current flows through L_{DIP} that causes a voltage drop on the output terminals. The values of L_{DIP}

and R_{DIP} had to be adapted for different dip depths at different loads to ensure that L_{DIP} has no significant effect on the terminal voltage when S_{DIP} is open. The dip generator used in the practical results operates on the same principle. The different loads that were used in the simulations to verify the dip compensation are shown in Figure 5.20.

5.8.1 Simulation of dip compensation

This part of the simulations was done for the various loads shown in Figure 5.20. Dip compensation was also simulated at different dip depths, but only for the resistive load.

a) Dip compensation with a resistive load

This compensation is illustrated in Figure 5.21 and Figure 5.22 for a dip with a depth of 16%. Figure 5.21 shows the effective compensation of the load voltage. Only three voltage steps have to be injected in each half cycle in the steady-state part of the dip for compensation (see Figure 5.22). The transients in the compensation at the beginning and end of the injected voltage are due to the controlled gradual adaptation of the load voltage to the phase shifts at the beginning and end of the dip. The few odd voltage steps in the beginning are due to the calculated amplitude and reference signal that are not established before the end of the first cycle. A solution for this simulation problem was found with the later simulations.

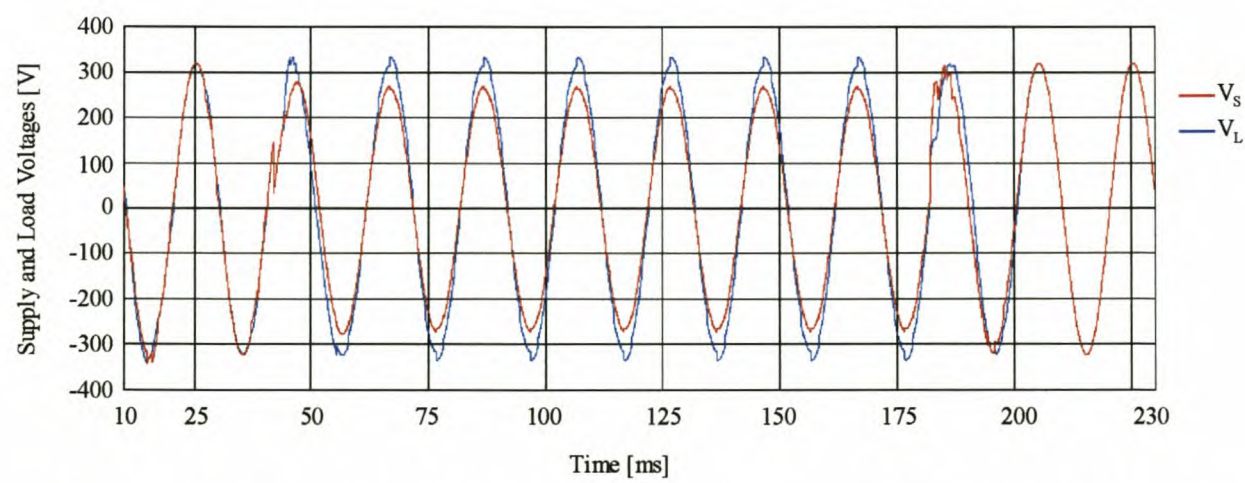


Figure 5.21: Phase voltages for resistive load dip compensation at a dip depth of 16%.

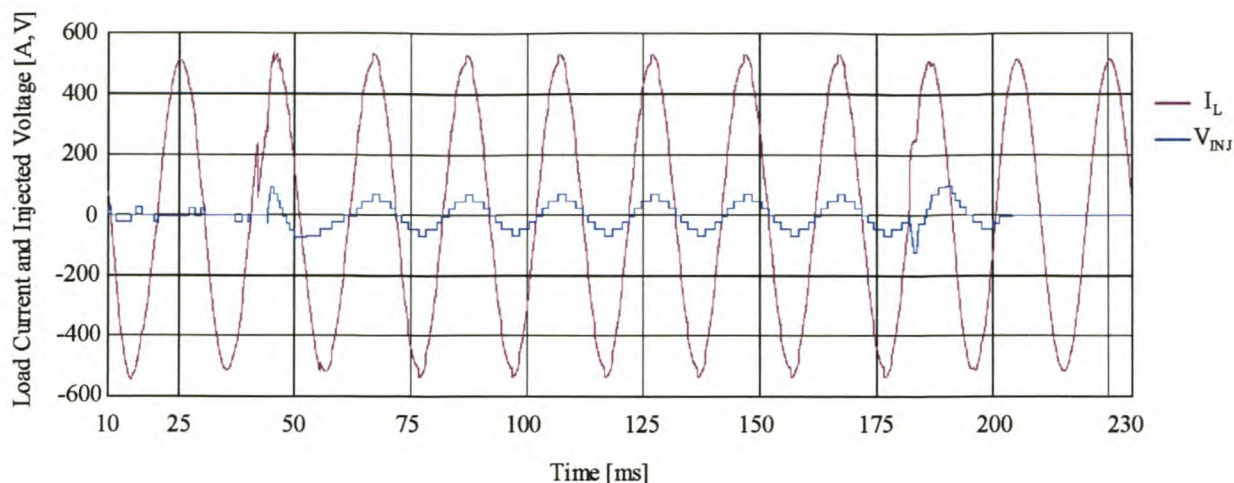


Figure 5.22: *Injected voltage and load current for resistive load dip compensation at a dip depth of 16%.*

The same kind of simulation was done for a dip with a depth of 52% in Figure 5.23 and Figure 5.24. This depth of 52% is more than the specified 30%. In spite of this the compensator still compensates for the dip, but with a slight drop in the load voltage (see Figure 5.23). The slight ripple in the load voltage, caused by the injected staircase voltage, is also visible. Figure 5.24 shows that five voltage steps are injected in each half cycle of the dip. This staircase voltage waveform has a very high modulation index, because it still tries to follow the error signal (see paragraph 5.4). The simulation proves the point that this compensator can provide limited compensation for dips deeper than the specified 30%.

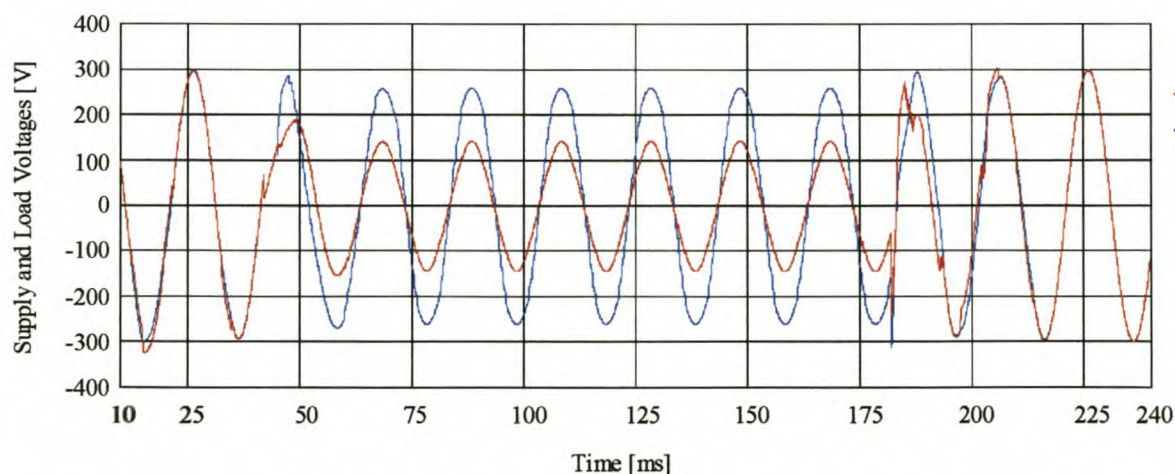


Figure 5.23: *Phase voltages for resistive load dip compensation at a dip depth of 52%.*

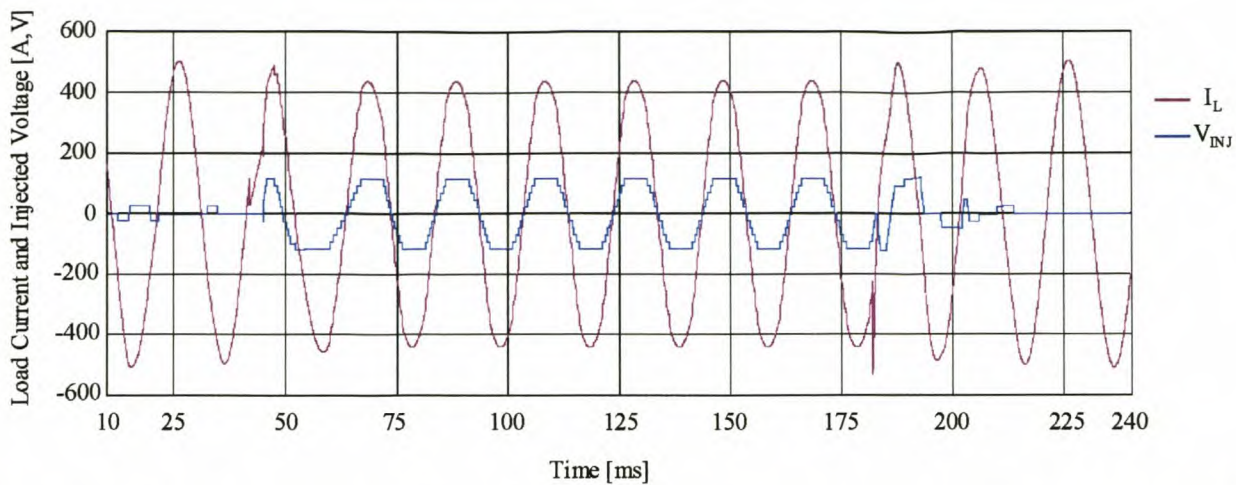


Figure 5.24: *Injected voltage and load current for resistive load dip compensation at a dip depth of 52%.*

Another simulation was done on the same load at the specified maximum depth of the dip and is shown in Figure 5.25 and Figure 5.26. It shows the effective compensation of the load voltage (Figure 5.25), due to the five voltage steps that are injected in each half cycle of the dip (Figure 5.26). There is even a slight rise in the load voltage. This can be ascribed to the insignificant voltage drop across the switching components that were accounted for in the design. The simulation in Figure 5.39 proves this ideal characteristic of the switching components in this simulation.

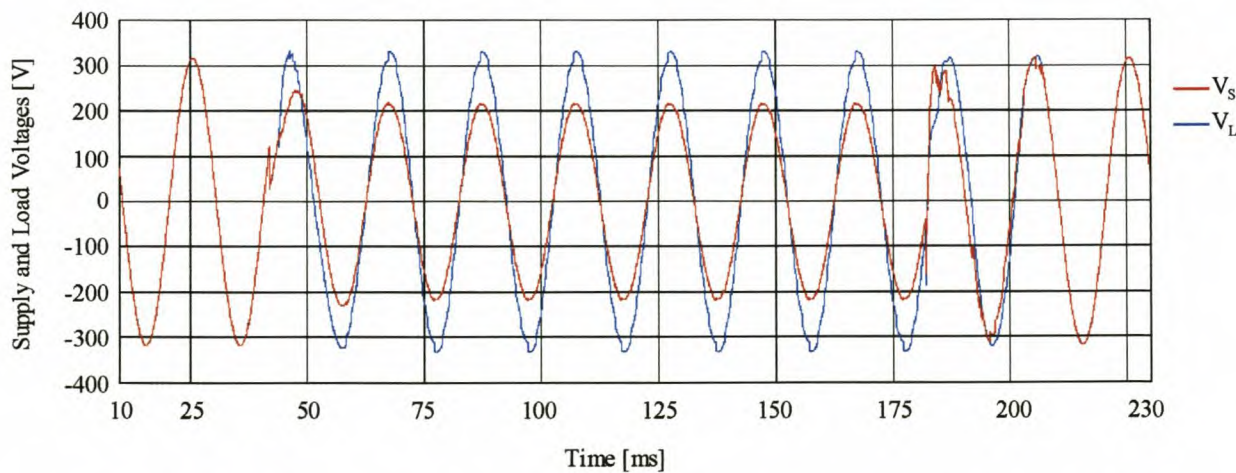


Figure 5.25: *Phase voltages for resistive load dip compensation at a dip depth of 30%.*

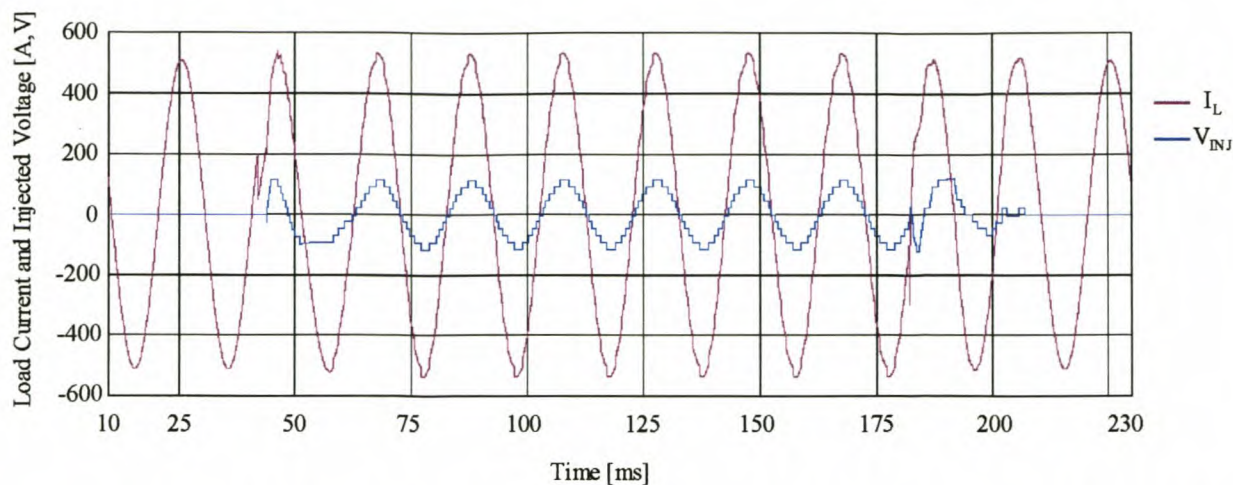


Figure 5.26: *Injected voltage and load current for resistive load dip compensation at a dip depth of 30%.*

b) Dip compensation with an inductive load

The same kind of simulation as the latter one was carried out on the inductive load in Figure 5.20 and is shown in Figure 5.27 and Figure 5.28. The displacement power factor of this load is $\text{DPF} = 0.6$ [G-10]. In Figure 5.27 the compensated load voltage shows not much difference from the load voltage in the case of the resistive load in Figure 5.25. Figure 5.28 clearly shows that the load current lags the injected staircase sinusoidal voltage waveform.

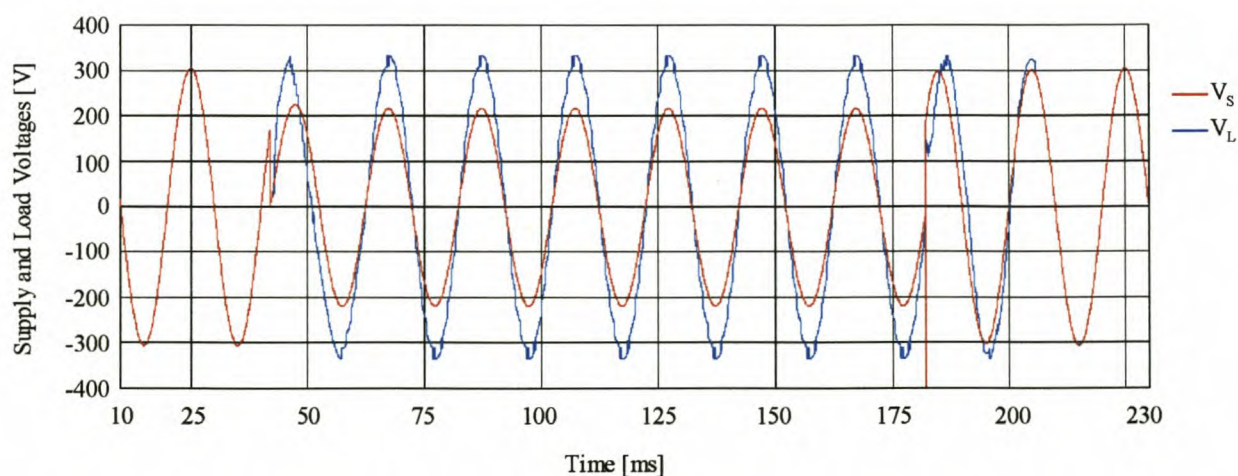


Figure 5.27: *Phase voltages for inductive load dip compensation at a dip depth of 30%.*

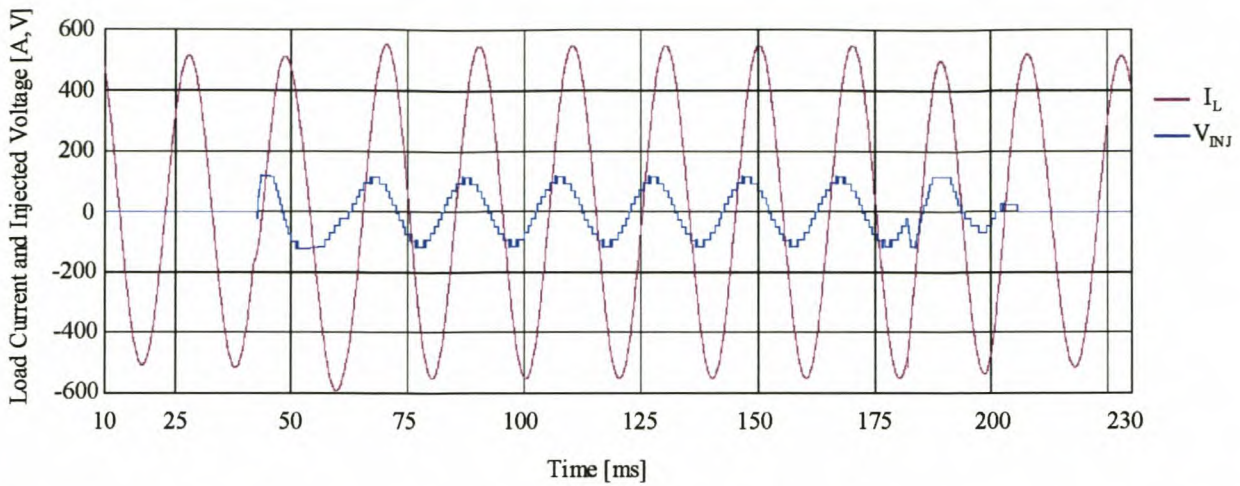


Figure 5.28: *Injected voltage and load current for inductive load dip compensation at a dip depth of 30%.*

c) Dip compensation with a non-linear load

A voltage dip with the same depth as in the latter two cases was simulated for the non-linear load in Figure 5.20. Figure 5.29 and Figure 5.30 display the compensation results for this simulation. The non-linearities in the supply voltage (V_s) are visible in Figure 5.29. The compensated supply voltage also shows not much difference from the latter two cases. The non-linear load current is shown in Figure 5.30. Slight notches on the positive rising and the negative declining edges of the load current are also visible during the dip. The reason for these notches is not known.

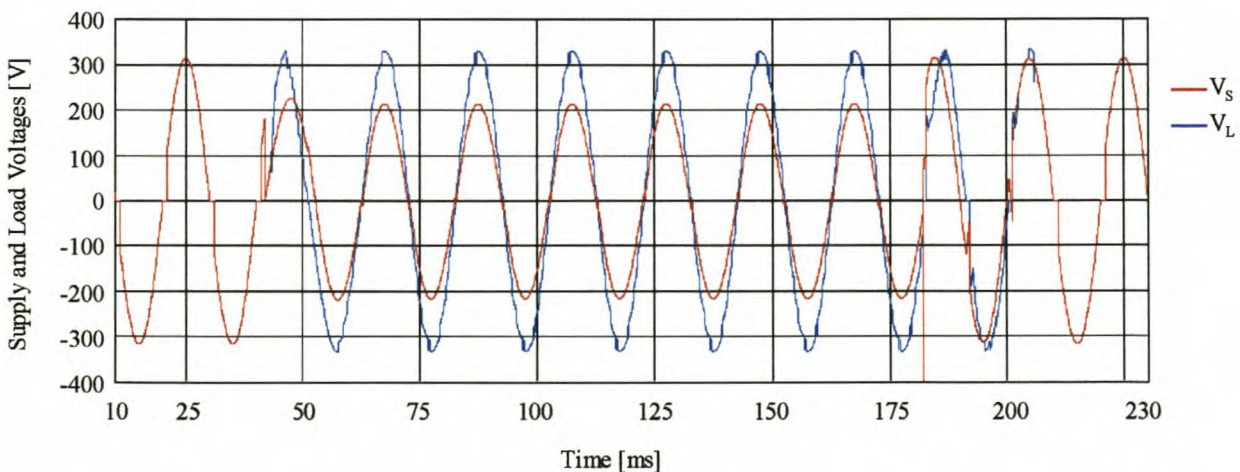


Figure 5.29: *Phase voltages for non-linear load dip compensation at a dip depth of 30%.*

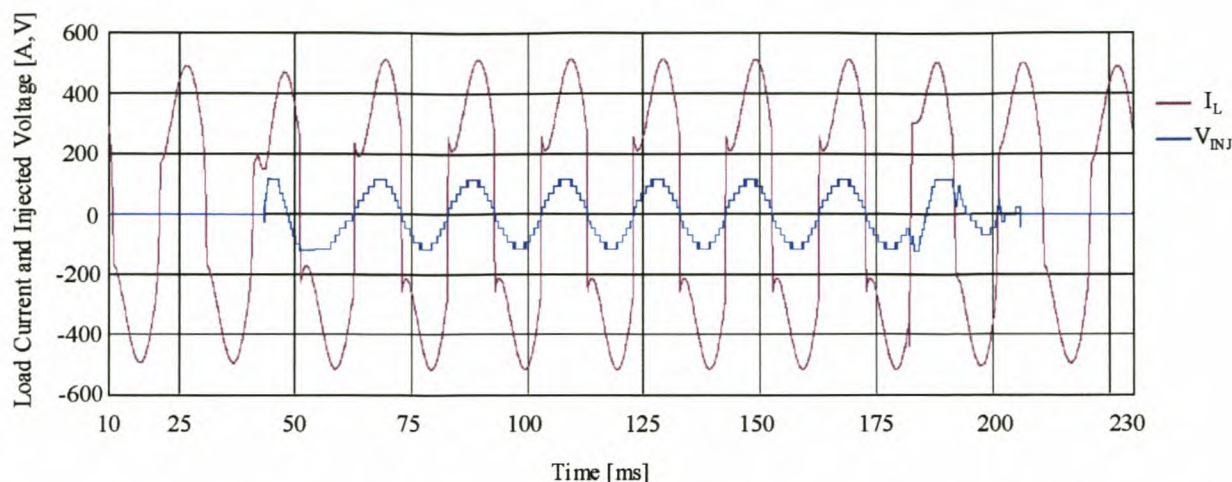


Figure 5.30: *Injected voltage and load current for non-linear load dip compensation at a dip depth of 30%.*

5.8.2 Verification of certain control techniques

a) *Sharing of the power dissipation*

A dip with a 16% depth was simulated for a resistive load to verify the above-mentioned control techniques. In this simulation (see Figure 5.21 and Figure 5.22) only three inverters delivered a voltage step in each half cycle in the ‘steady-state’ part of the dip. This simulation is therefore a good example of the implemented sharing technique. Figure 5.31 and Figure 5.32 show the integrated values of the square of the currents during the dip delivered by the DC buses and also conducted by the switches of one of the inverters, respectively. The increase in these values after the end of the dip at 182 ms is caused by the transient in the compensation, resulting from the phase shift at the end of the dip.

Even though each DC bus did not deliver current during each half cycle, Figure 5.31 shows an overall simultaneous increase in the integrated squared values of the currents. It verifies therefore the sharing of the power dissipation in the DC buses.

If each DC bus does not deliver current during each half cycle, two DC buses will have a zero output during each half cycle. In spite of this Figure 5.32 still shows an overall simultaneous increase in the power dissipation in all the switches for one of the inverters. Figure 5.33 shows that the result in Figure 5.32 is almost the same for all the switches in all the individual inverters of the multilevel inverter.

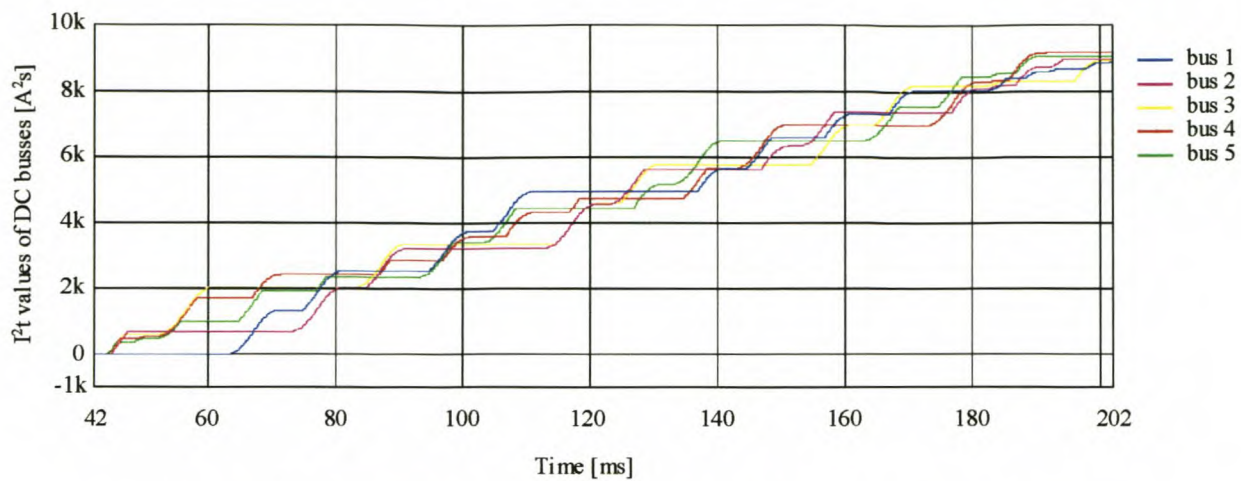


Figure 5.31: Simulated sharing of the power delivery of the DC buses.

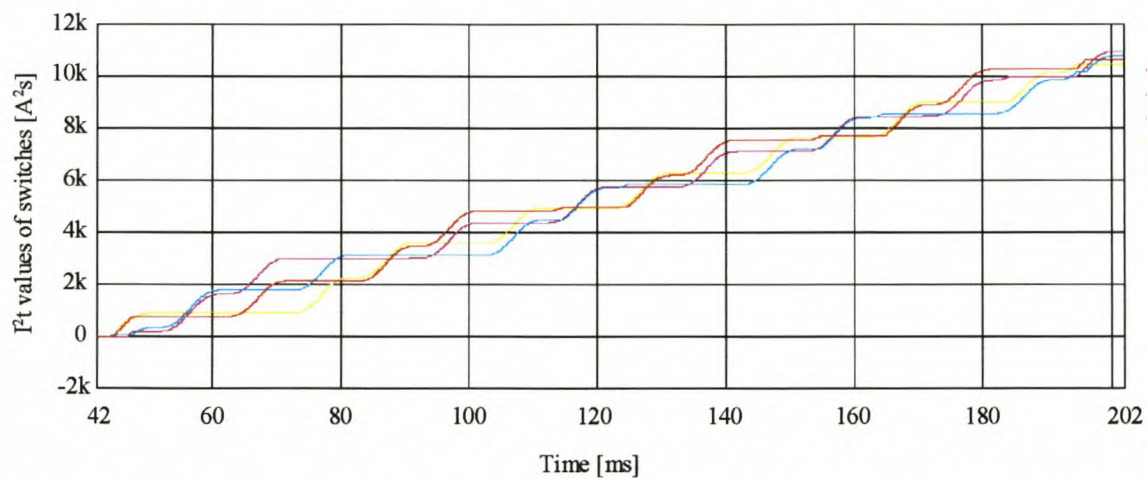


Figure 5.32: Simulated sharing of the power dissipation in the switches in one of the inverters.

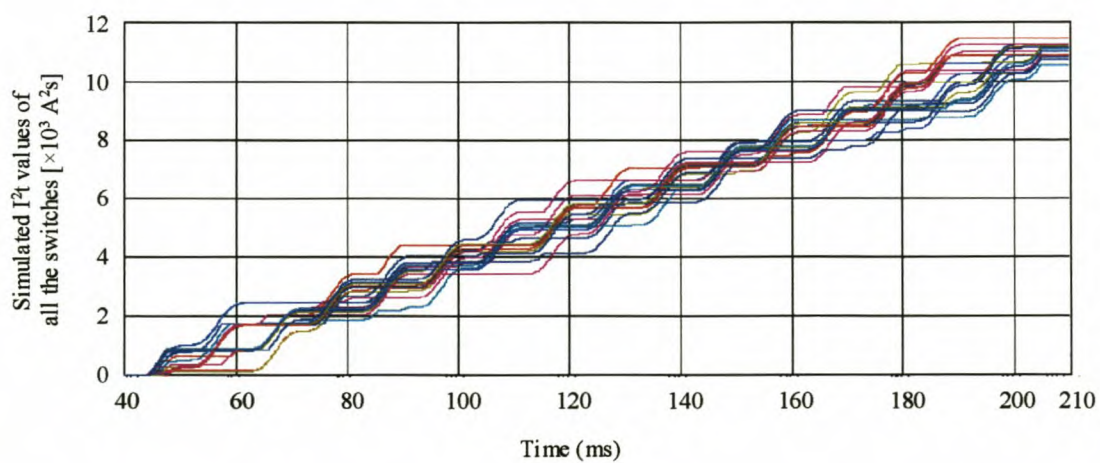


Figure 5.33: Simulated estimation of the integrated power dissipation in all the switches of the multilevel inverter.

These figures show that sharing of the power dissipation in the batteries and the MOSFETs can be achieved simultaneously.

b) Force commutation

This method, as explained in 5.7.1 and illustrated in Figure 5.18, is verified in Figure 5.34 for a resistive load. For this simulation a small inductance of 0.5 μ H was added in series with the terminals of the multilevel inverter to make this simulation more realistic. The figure below gives a close look at the voltage pulses across the thyristor (V_{INJ}), together with the thyristor current (I_{THY}) at the same time. The thyristor current shows a decrease after the first pulse and it terminates almost immediately at the beginning of the second pulse.

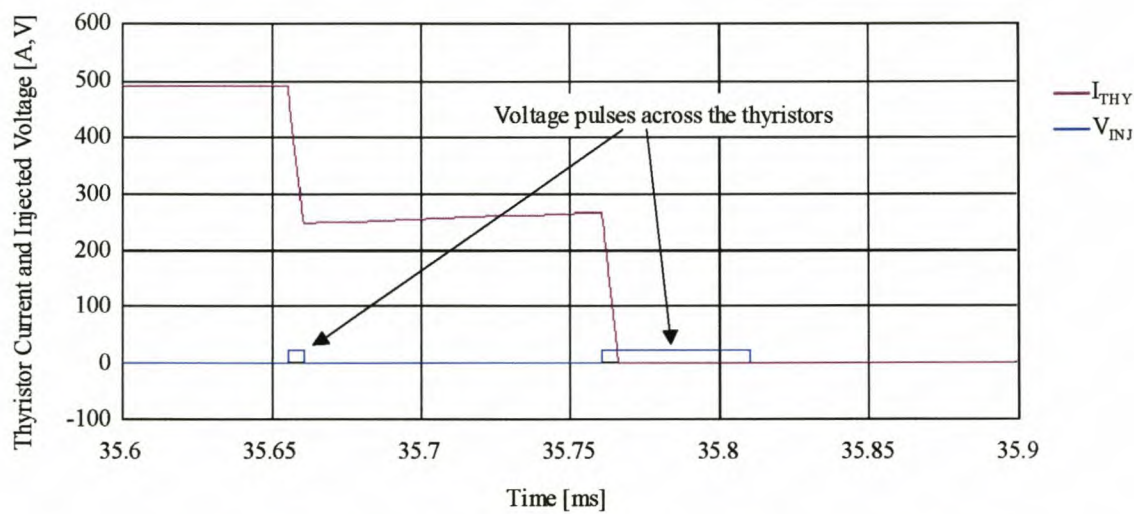


Figure 5.34: *Simulated illustration of the force commutation method.*

The above method was also simulated with the inductive load in Figure 5.20. This load has a displacement power factor (DPF) of 0.6 [G-10]. Figure 5.35 and Figure 5.36 show the force commutation for the two conditions where the voltage and current polarities are the same. The simulations of the force commutation in the time period t_p . (see Figure 5.16) when the polarities differ are shown in Figure 5.37 and Figure 5.38. All of these simulations show that the thyristor current comes to an abrupt end. They also show the phase jump in the supply voltage at the beginning of the dip very clearly.

The condition where the force commutation takes place at the zero-crossing of the current could not be properly verified, because the thyristors in the simulation have very ideal characteristics.

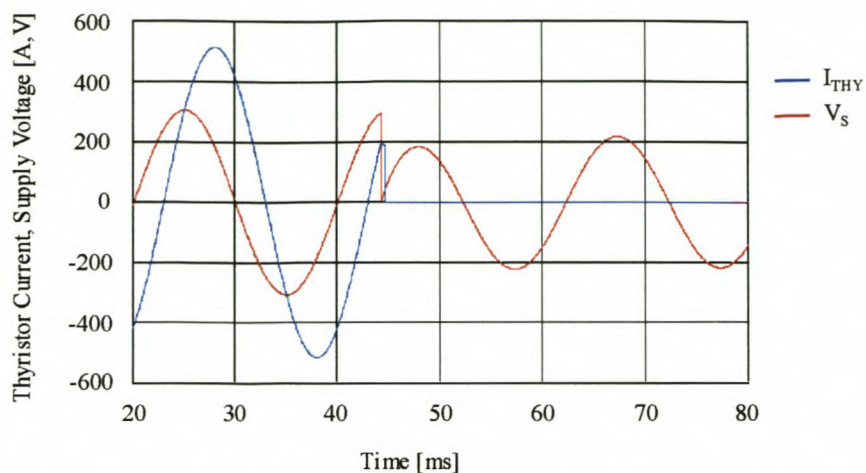


Figure 5.35: Force commutation where $V_S > 0$ and $I_{THY} > 0$.

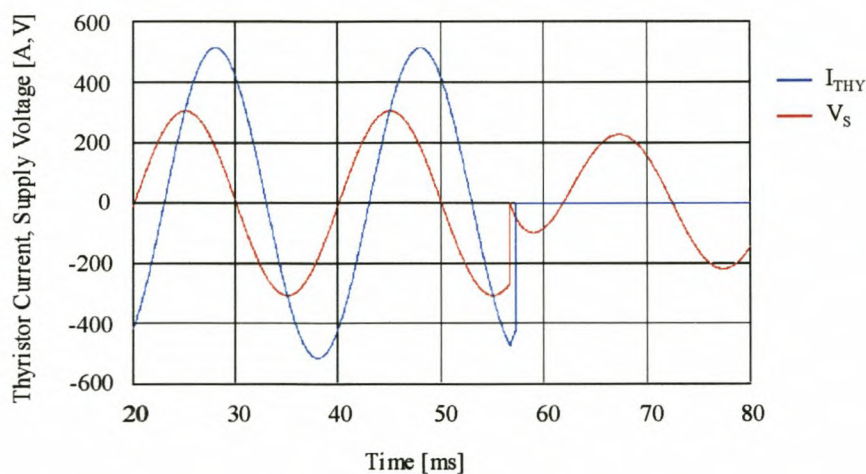


Figure 5.36: Force commutation where $V_S < 0$ and $I_{THY} < 0$.

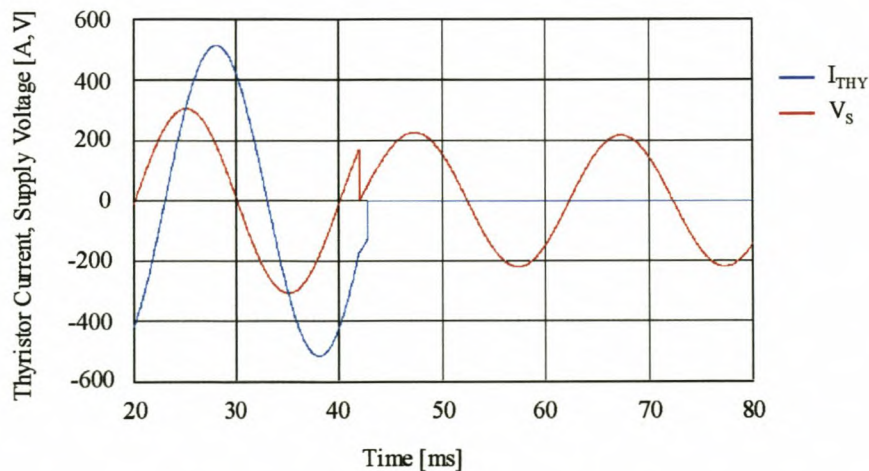


Figure 5.37: Force commutation where $V_S > 0$ and $I_{THY} < 0$.

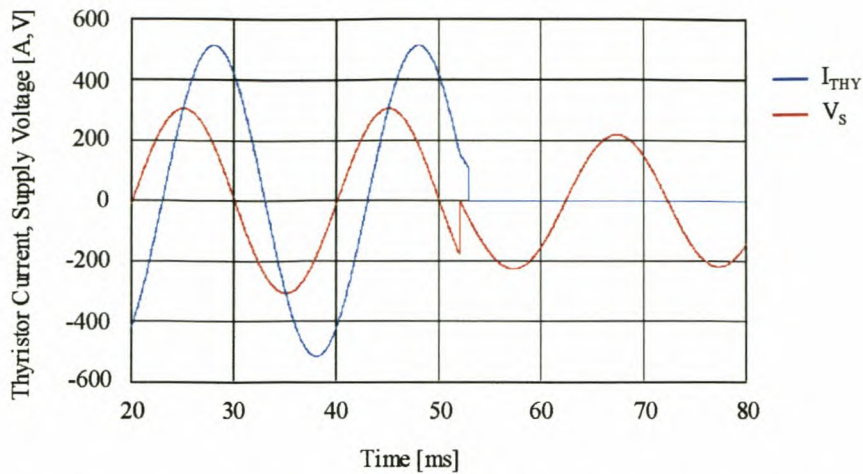


Figure 5.38: Force commutation where $V_S < 0$ and $I_{THY} > 0$.

c) Staircase sine waveform

A simulation of the staircase sine waveform with the multilevel inverter only is shown in Figure 5.39. It shows the output voltage of the multilevel inverter (V_{INJ}) together with the 50 Hz reference signal (V_{REF}). It was simulated at rated current with a resistive load in exactly the same way as the one in Figure 3.3. The reason for the ideal voltage steps of almost 24 V can be ascribed to the low voltage drop across the switching components with very ideal characteristics. In the practical results the size of the voltage steps should fall at least with 1.22 V.

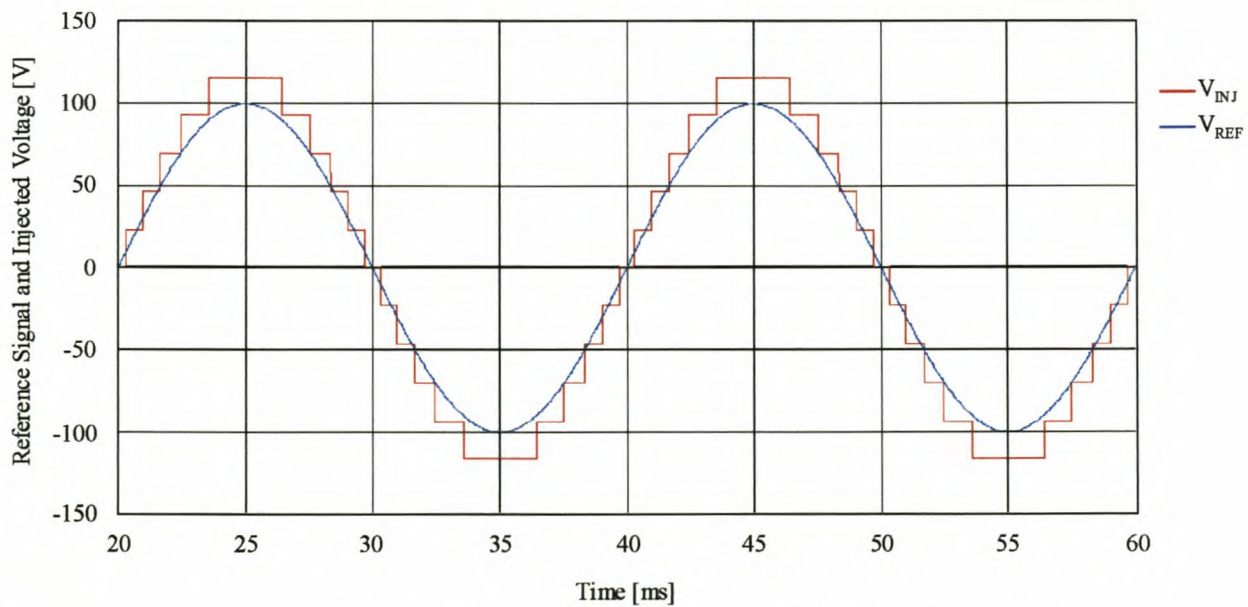


Figure 5.39: Staircase sine waveform.

Summary

This chapter discussed the control methods of the multilevel inverter for series dip compensation. Existing control techniques were evaluated to obtain the best possible techniques for dip detection and synchronisation for single-phase dip compensation. The $\frac{1}{4}$ cycle relationship and the DFT synchronising techniques were chosen for dip detection and synchronisation respectively. In the latter method the reference signal gradually adapts to the phase shifts at the beginning and end of the voltage dip. The way in which voltage steps are added to the supply voltage is based on existing techniques. The existing techniques are based on the assumption of a relative steady-state output voltage, which is not the case for the transient nature of voltage dips. Because of this a new technique for the sharing of the power dissipation in the switches and the batteries had to be developed, based on existing techniques. Finally, the control of the thyristors in the initiation and termination of dip compensation and the fault current protection was discussed. A new method for force commutation of the thyristors was also developed. Most of the control methods were confirmed with simulations in Simplorer.

6. Practical results

6.1 Introduction

The simulations in Chapter 5 gave an indication of the multilevel inverter's ability to compensate for dips when it is directly coupled in series with a power line. A scale model of the multilevel inverter (at rated voltage, but with a small load current) was built at first to verify the control methods for dip compensation. Phase arms used for undergraduate courses were used to build up this multilevel inverter. The scale model dip compensator proved to be successful and the results are given in Appendix D.

A single inverter of the full-scale model was then built and tested before the whole multilevel inverter was constructed, as explained in Chapter 4. The important results of the single inverter and the full-scale multilevel inverter are discussed in this chapter. (The rest of the results are also included in Appendix D.)

Paragraph 6.2 gives the results for the single inverter, together with the voltage overshoot across the MOSFETs at turn-off. The dip compensation results on resistive, inductive and non-linear loads are represented in almost the same way as the simulations in paragraph 6.3. Finally the new methods of force commutation and sharing of the power dissipation are verified practically in paragraph 6.4. This chapter also concludes with a summary.

6.2 Tests on a single inverter

The single inverter that was built at first was tested on a resistive load by switching a three-level staircase voltage waveform to the output. This waveform was synchronised with a 50 Hz sinusoidal signal and it was controlled to last for a period of 500 ms. The experimental set-up is shown in Figure 6.1. The staircase waveforms for the output voltage and the load current, with a 360 A amplitude, are displayed in Figure 6.2. The gradual transitions in the current are caused by the stray inductances in the bus bars and also a small inductance in the load. The internal resistance of the batteries, which could not be determined beforehand, caused the decrease in the output voltage.

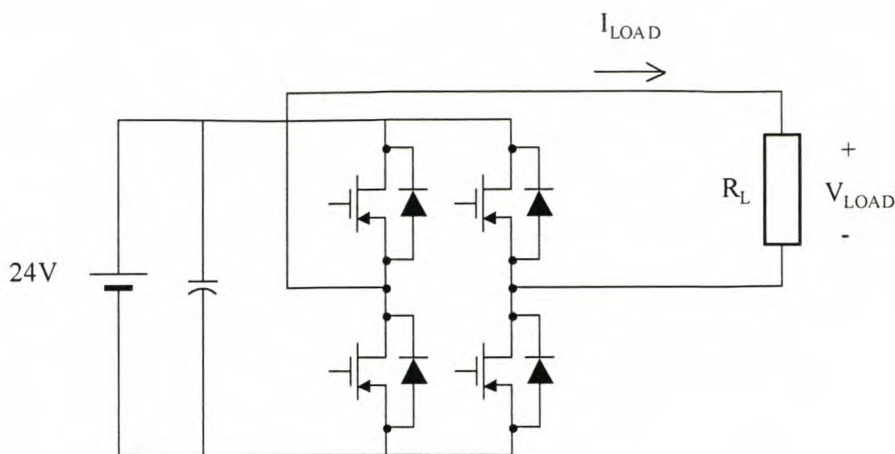


Figure 6.1: Experimental set-up for the tests on the single inverter.

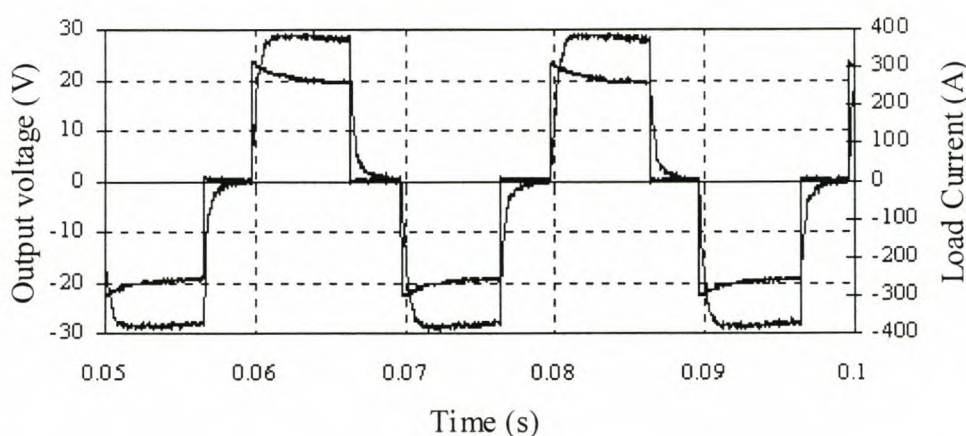


Figure 6.2: Square wave load voltage and current for a single inverter.

It is a well-known fact that semiconductor switches are very sensitive to over-voltages. Voltage peaks occur at turn-off and are caused by the stray inductances in the bus bars and connections. The amplitudes of these peaks therefore depend on the instantaneous value of the load current. Figure 6.3 shows the voltage V_{DS} across the MOSFETs at the turn-off transient for the above 360 A load current. The peak value of V_{DS} (40.6 V) is still much less than the maximum rated value of the MOSFETs at 60 V. This inverter was tested for increasing values of the load current to verify the possible maximum voltages across the MOSFETs. Figure 6.4 is a plot of the maximum voltage across the MOSFETs (V_{DSmax}) at turn-off versus the instantaneous value of the load current. The measured experimental values are represented as dots and are interpolated to predict the maximum voltages at higher currents. The maximum theoretical instantaneous value of the load current will be the amplitude of the rated load current (360 A_{RMS}) at 509 A. According to the interpolating line, this load current will not cause V_{DSmax} to get out of bounds.

The on-state voltage of the MOSFETs could not be accurately determined, because the oscilloscope used in the measurements has a very small voltage offset. From the above measurements, however, it seems that the maximum on-state voltage of the MOSFETs $V_{DS(on)}$ is round about the expected value of 0.61 V.

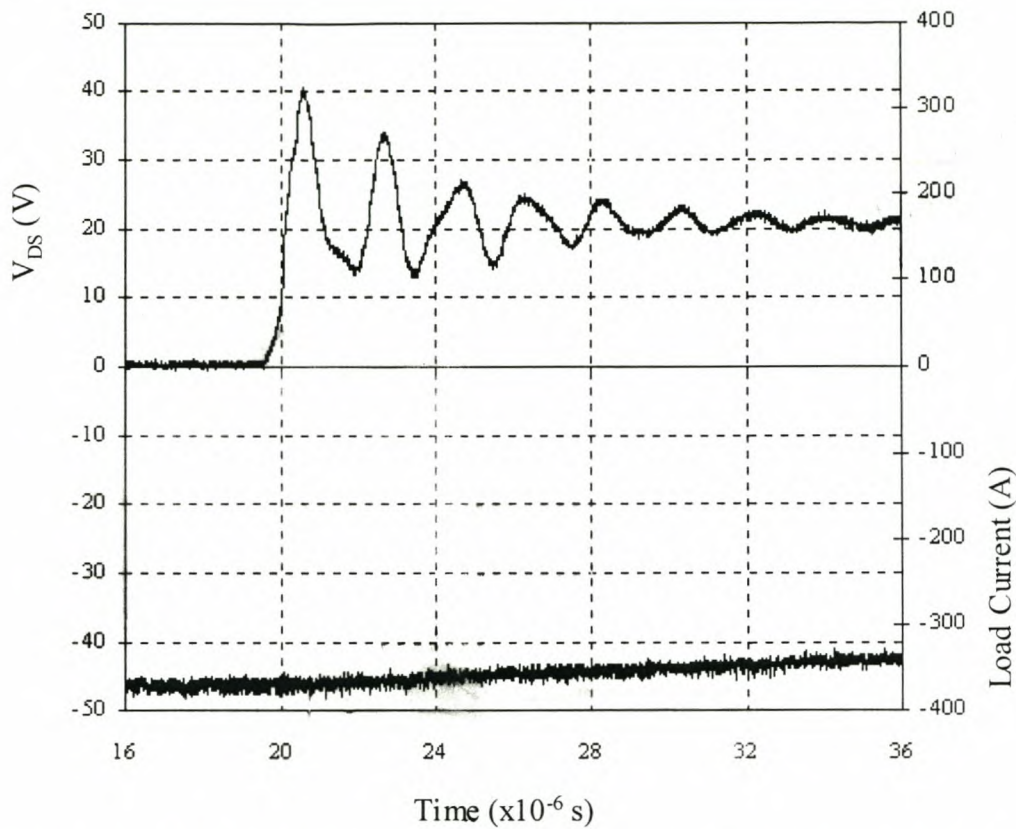


Figure 6.3: Drain-source voltage of the MOSFETs at turn-off for a load current of 360 A.

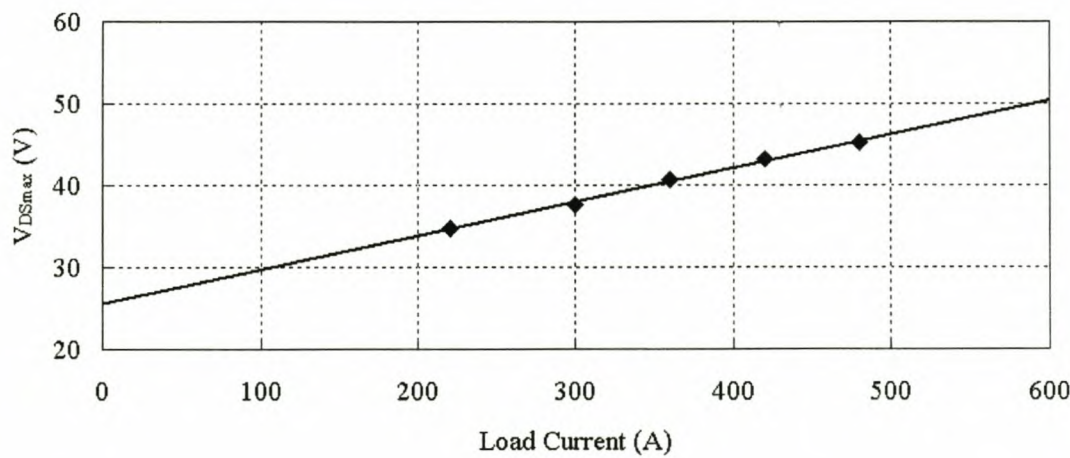


Figure 6.4: Plot of peak drain-source voltage versus load current for a single inverter.

6.3 Dip compensation results with the multilevel inverter

These results were taken for various loads by using a dip generator developed at the University of Stellenbosch. The experimental set-up, including the dip generator configuration, is shown in Figure 6.5 with the basic parameters in Table 6.1. This dip generator works on the same principle as the one in the simulations in Figure 5.19. The compensation is also tested for the same types of loads (resistive, inductive, non-linear) in Figure 5.20. It was difficult to set the dip generator and loads for specific depths of dips at the specified load current and dip depths. A significant voltage drop across the dip generator’s inductor L_{DIP} at the higher currents, when no dip was present, also caused the measured supply voltage to be lower than specified. The dip generator’s resistance R_{DIP} was also limited by the thyristors’ current rating to a minimum value of $0.4\ \Omega$. In spite of these shortcomings the following results clearly indicate that this multilevel inverter is fully capable of compensating the dips as specified in paragraph 4.2.

Table 6.1: Basic parameters for the above experimental set-up.

| Parameter | Value |
|--|-------------------------------|
| Supply voltage (V_S) | 220 V _{RMS} |
| Line frequency | 50 Hz |
| Dip duration | About 10 cycles (207 ms) |
| Line inductance (L_{DIP}) | 0.1/ 0.2/ 0.4/ 0.8/ 1.2 mH |
| Short-circuit resistance (R_{DIP}) | 0.4 Ω |

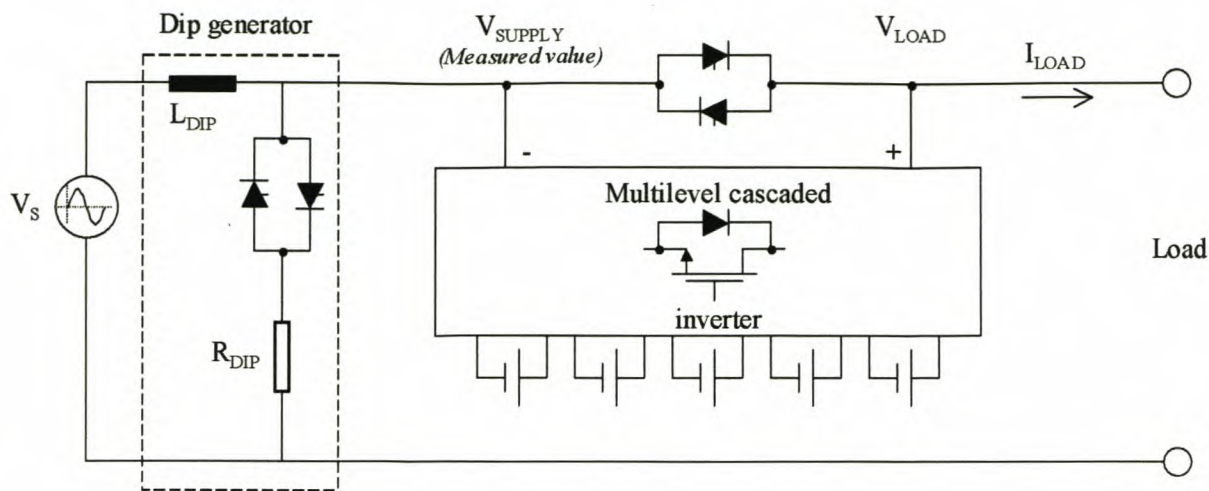
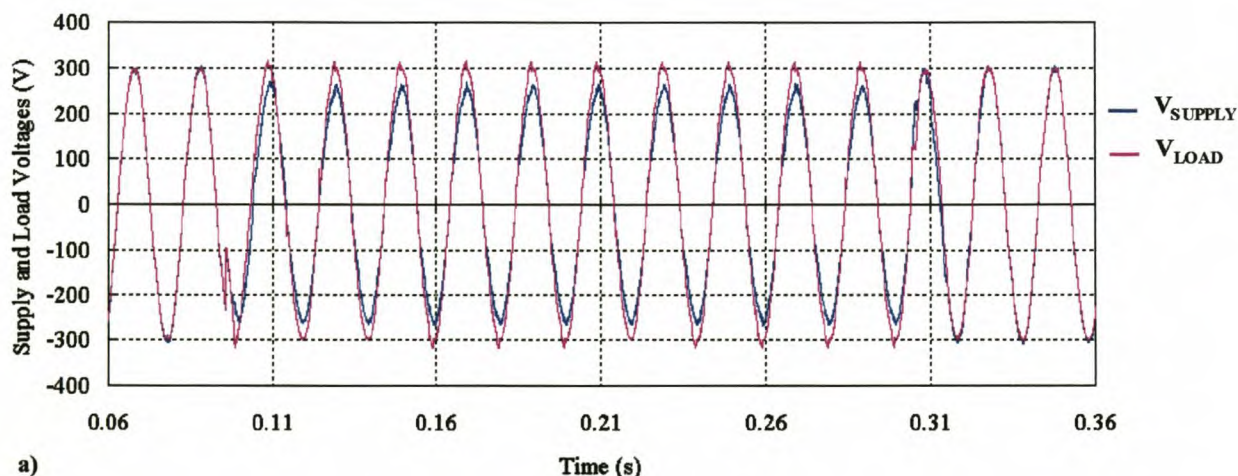


Figure 6.5: *Experimental set-up for the dip compensation results.*

6.3.1 Dip compensation with a resistive load

Dip compensation for this load was tested at first for dips at various depths with a $1\ \Omega$ load resistance. The first test was for a dip at a small depth of 13% and a $230\text{ A}_{\text{RMS}}$ load current, where $L_{\text{DIP}} = 0.4\text{ mH}$. The results are shown in Figure 6.6 a) and b). These results look very similar to the ones in Figure 5.21 and Figure 5.22 for the same type of load at a dip depth of 16%. Figure 6.6b also shows that only three voltage steps have to be injected in each half cycle in the steady-state part of the dip. The same types of transients in the injected voltage, caused by the phase jumps at the beginning and end of the dip, are also present.



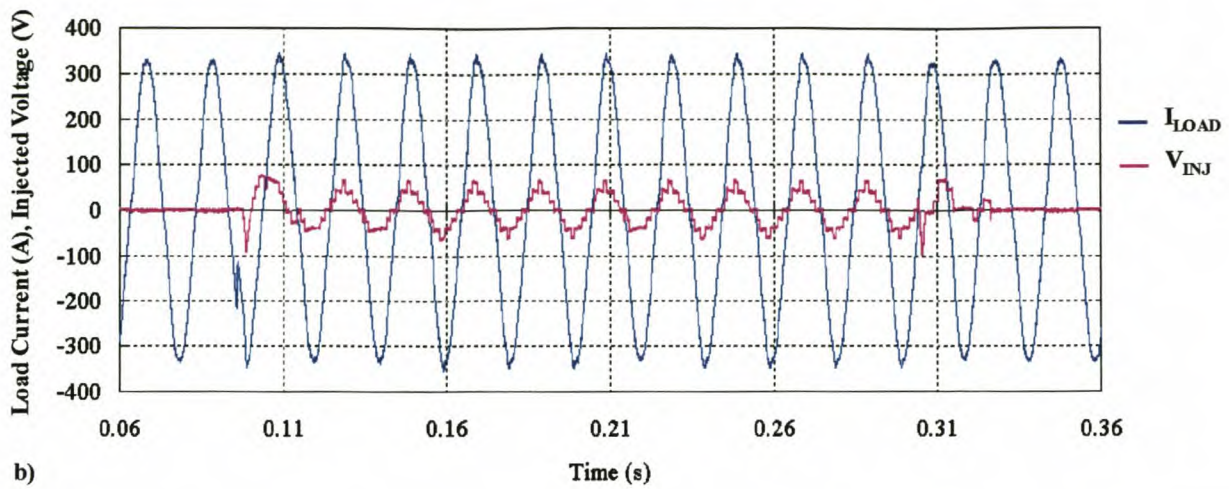
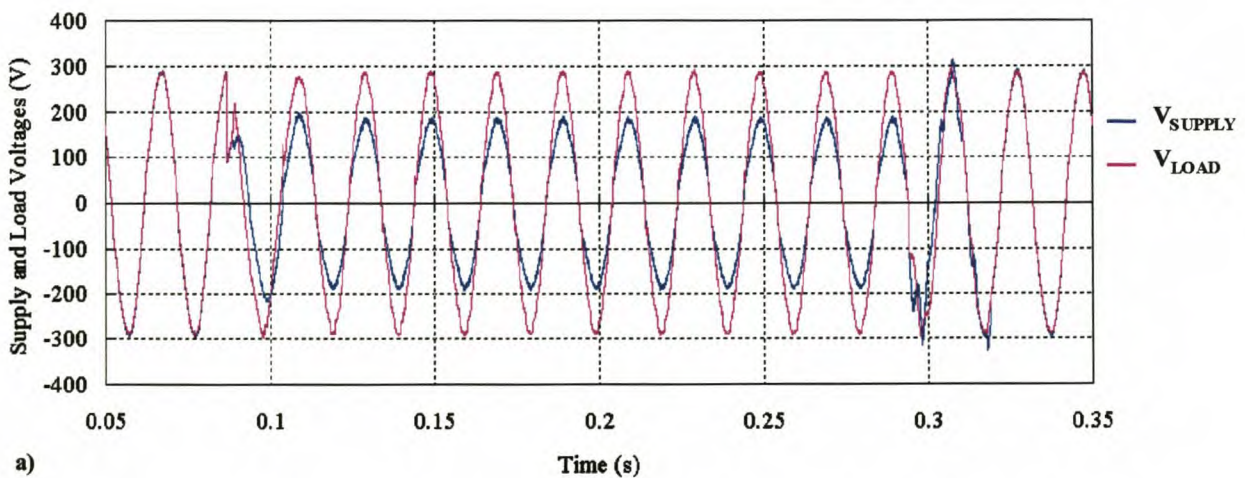


Figure 6.6: Dip compensation on a 13% dip for a resistive load at 230 A_{RMS} : a) Load and supply voltages, b) Load current and injected voltage.

Figure 6.7 shows dip compensation for the same load resistance at a dip depth of 34% ($L_{DIP} = 0.8$ mH) and a load current of 213 A. This result clearly shows this system's capability to compensate fully for dips up to the specified depth with five voltage steps in each cycle of the injected voltage. A slight ripple in the load voltage can be seen in the zoomed view (Figure 6.8) of Figure 6.7, caused by the injected voltage. Figure 6.8 b) also clearly shows that the voltage steps are round about 20 V. This is caused by the voltage loss across the MOSFETs and the internal resistance of the batteries. The simulations showed 24 V steps, which was quite ideal.



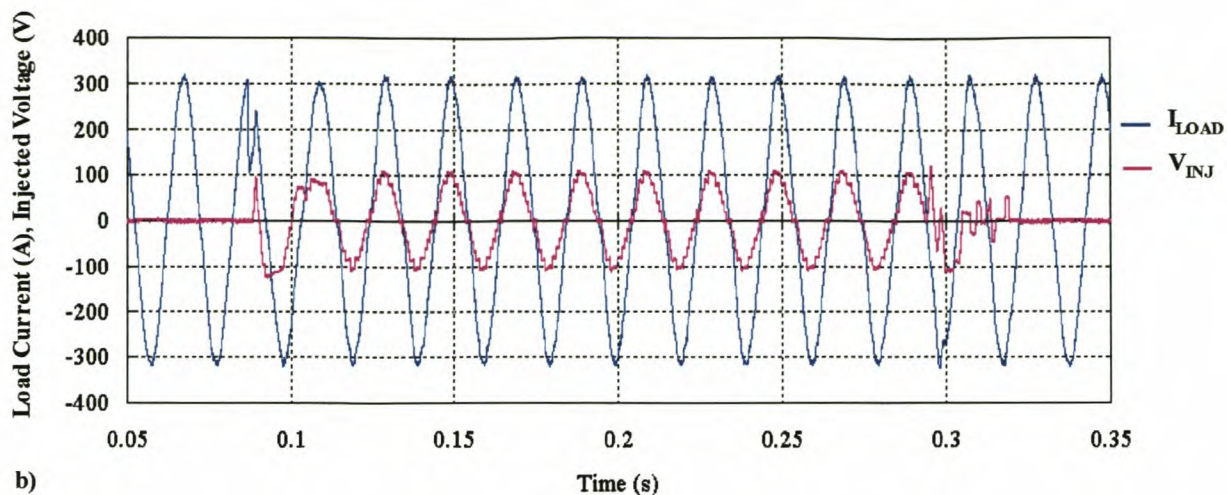


Figure 6.7: Dip compensation on a 34% dip for a resistive load at 213 A_{RMS} : a) Load and supply voltages, b) Load current and injected voltage.

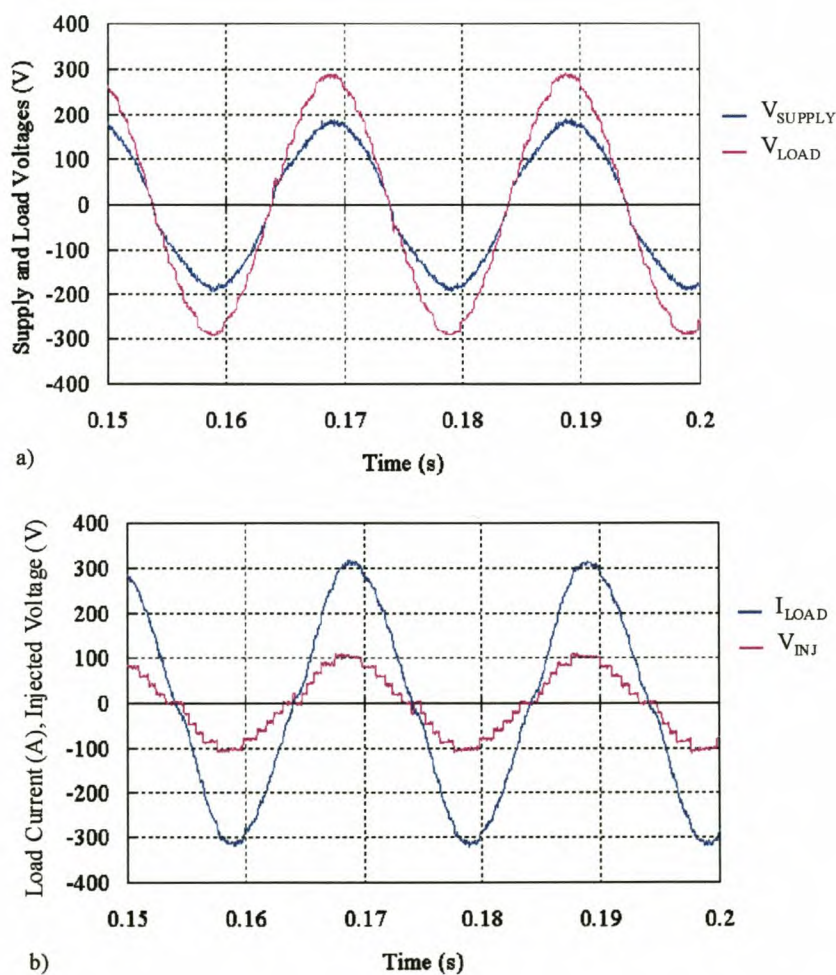


Figure 6.8: Zoomed view of the waveforms from a) Figure 6.7a and b) Figure 6.7b.

The dip compensation result for a dip at a depth of 50% ($L_{DIP} = 1.2\text{mH}$) at a load current of 208 A_{RMS} is shown in Figure 6.9. This result verifies the simulation in Figure 5.23 and Figure 5.24. It clearly shows the compensator's capability to provide limited compensation for dips deeper than the specified depth of 30%.

It was stated in the beginning that the results in Figure 6.6 - Figure 6.9 were taken with the same load resistance of 1 Ω . The reason for the difference in load current is the difference in the voltage drop across the inductor L_{DIP} of the generator that causes a difference in the supply voltage.

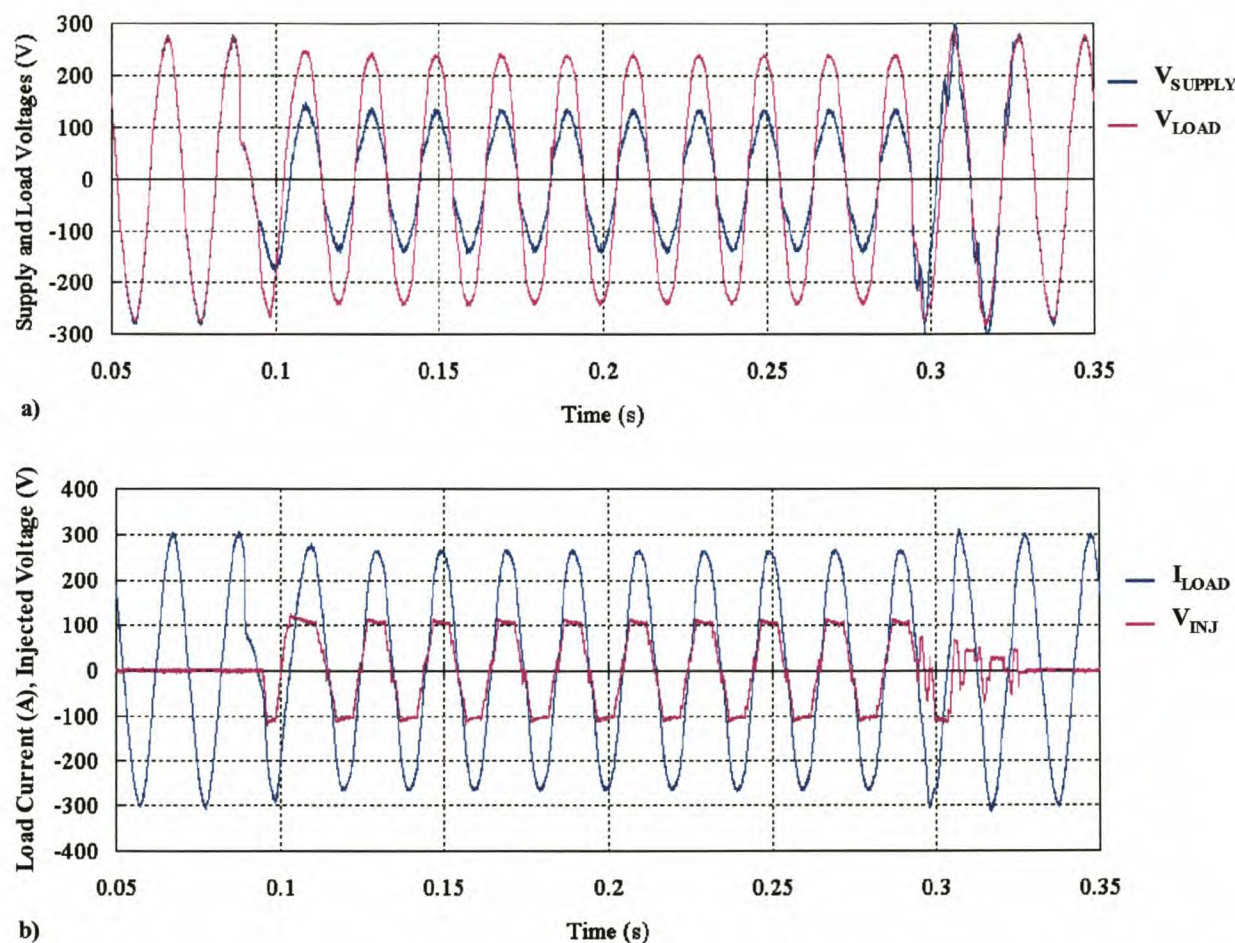


Figure 6.9: Dip compensation on a 50% dip for a resistive load at 208 A_{RMS} : a) Load and supply voltages, b) Load current and injected voltage.

One result was taken at almost the full rated current to verify the compensator's performance for this specification. Figure 6.10 shows dip compensation at a 350 A_{RMS} load current at a dip depth of 41%. A load resistance of 0.5 Ω was used with $L_{DIP} = 0.8\text{mH}$. The 41% dip depth explains the slight drop in the load voltage. The slight decrease in the amplitude at the top stairs of the injected voltage, caused by the internal resistance of the batteries, is also evident.

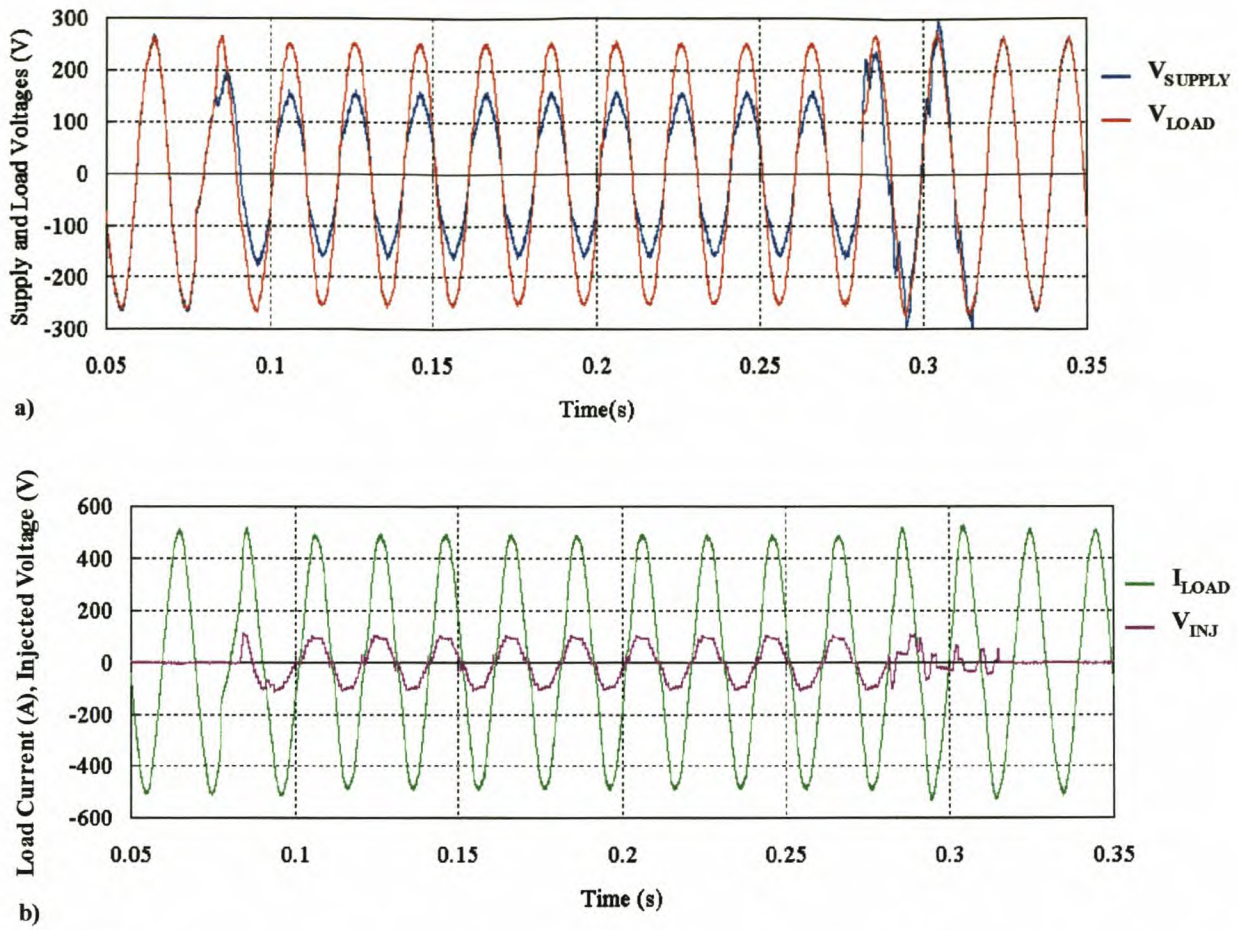


Figure 6.10: Dip compensation on a 41% dip for a resistive load at 350 A_{RMS} : a) Load and supply voltages, b) Load current and injected voltage.

The voltage overshoot across the MOSFETs was measured again for the multilevel inverter as in the case of the single inverter (Figure 6.3). This result is shown in Figure 6.11 for a current of 441 A. The measured values of the maximum voltage across the MOSFETs at turn-off (V_{DSmax}) versus the load current for the multilevel inverter are plotted again in Figure 6.12. These values are slightly higher than the ones in Figure 6.4. This is due to the inductance in the cables that connect the individual inverters' outputs. Also note that the battery voltage also plays a role in the value of V_{DSmax} . This voltage will depend on how much the batteries have been discharged at that stage and also on the switching state before turn-off, i.e. if the inverter was in the zero state (states 1 and 3 of Figure 5.14) or not.

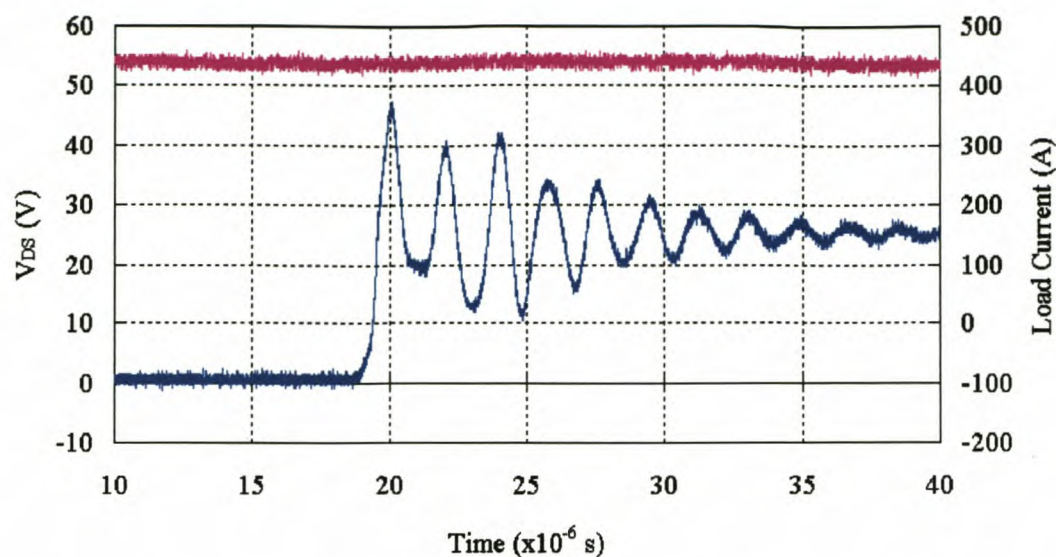


Figure 6.11: Drain-source voltage of the MOSFETs at turn-off for a load current of 441 A.

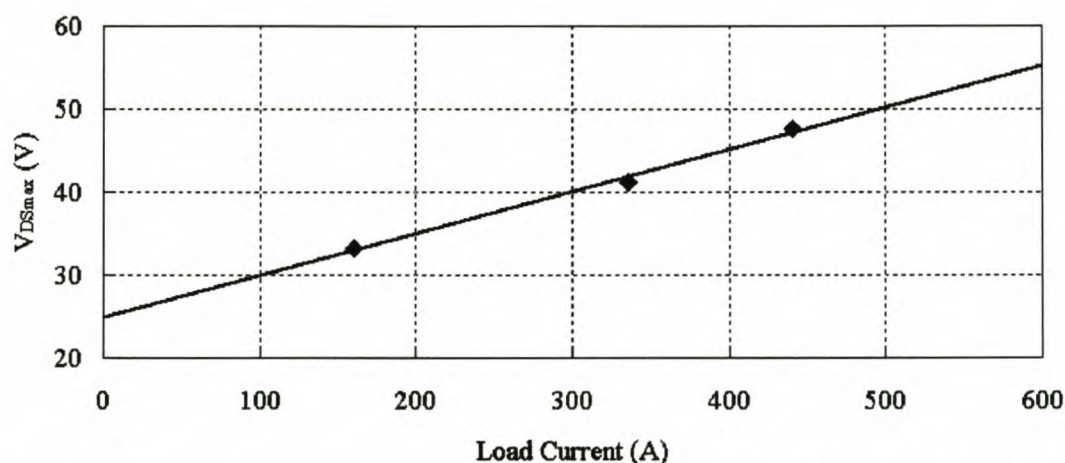


Figure 6.12: Plot of peak drain-source voltage versus load current for the multilevel inverter.

6.3.2 Dip compensation with an inductive load

This experimental set-up caused a very large voltage drop across L_{DIP} when no dip was present. The depth of the dips was also limited. The dip result (depth = 27%) in Figure 6.13 still proves that this compensator is able to compensate for dips for this type of load. This test was done on an inductive load with a displacement power factor of 0.54 at a 200 A_{RMS} load current. The parameters of the load and the dip generator are as follows: $R_L = 0.35 \, \Omega$, $L_L = 1.8 \, \text{mH}$ and $L_{DIP} = 0.8 \, \text{mH}$. Figure 6.13 b) clearly shows the phase difference between the load current and the injected voltage.

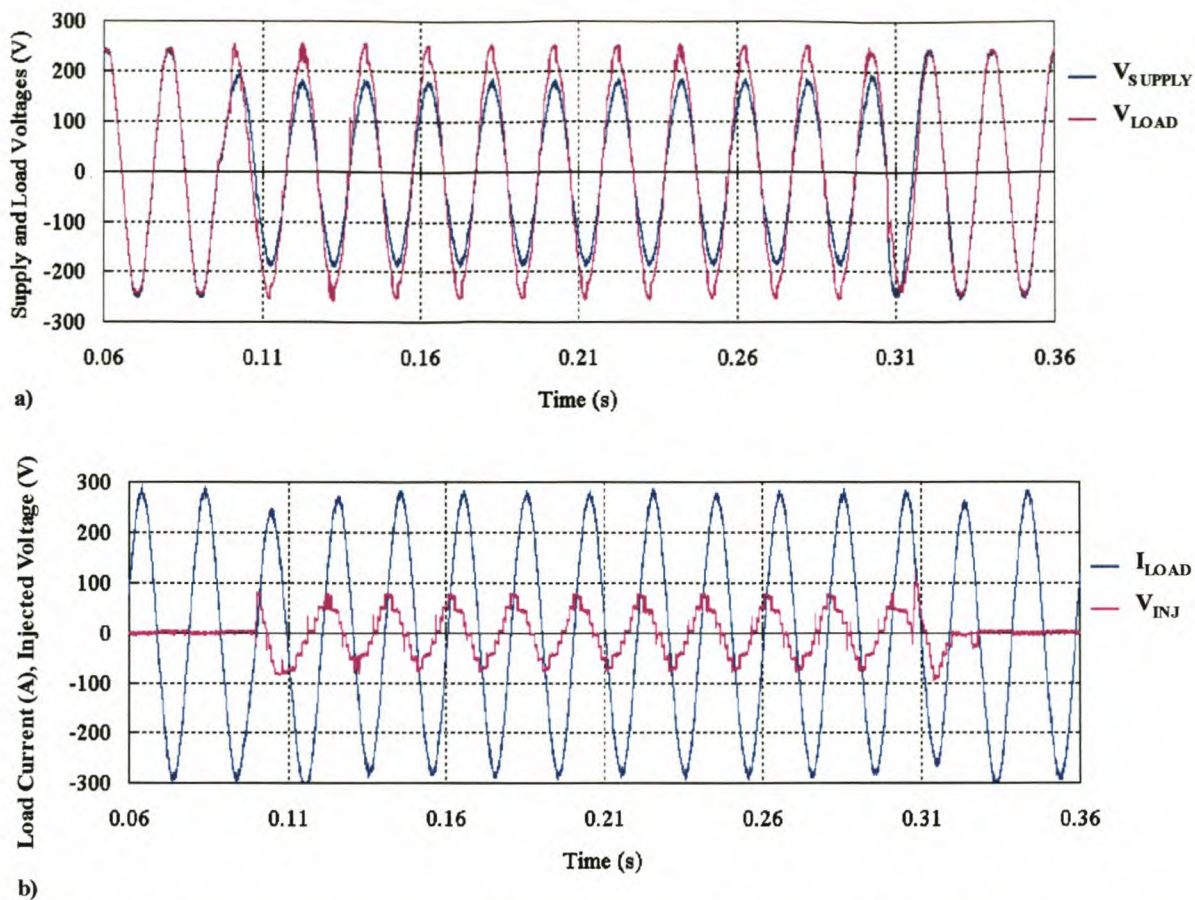


Figure 6.13: Dip compensation on a 27% dip for an inductive load at 200 A_{RMS}: a) Load and supply voltages, b) Load current and injected voltage.

6.3.3 Dip compensation with a non-linear load

It is very important to verify that this compensator can compensate for non-linear loads. Non-linear loads comprise quite a large part of the total load on electric lines. Examples of non-linear loads are domestic lights, ovens, TVs, computer power supplies, air conditioners, laser printers and photocopiers [S-6]. The experimental set-up for this load was the same as the one in the simulations with the same values of R_L , L_L and L_{DIP} as in the case of the previous result. The compensation result for this dip at a depth of 38% for a non-linear load at a 340 A_{RMS} load current is represented in Figure 6.14. The non-linearities in the supply voltage before the start of the dip are clearly visible. The reason for the sharp notches in the supply voltage during the dip is uncertain. They might be caused by the combined effect of the thyristors in the dip generator and the diodes of the non-linear load. The dip compensator, though, compensates for this effect. Figure 6.14 b) also clearly shows the non-linear effect on the load current.

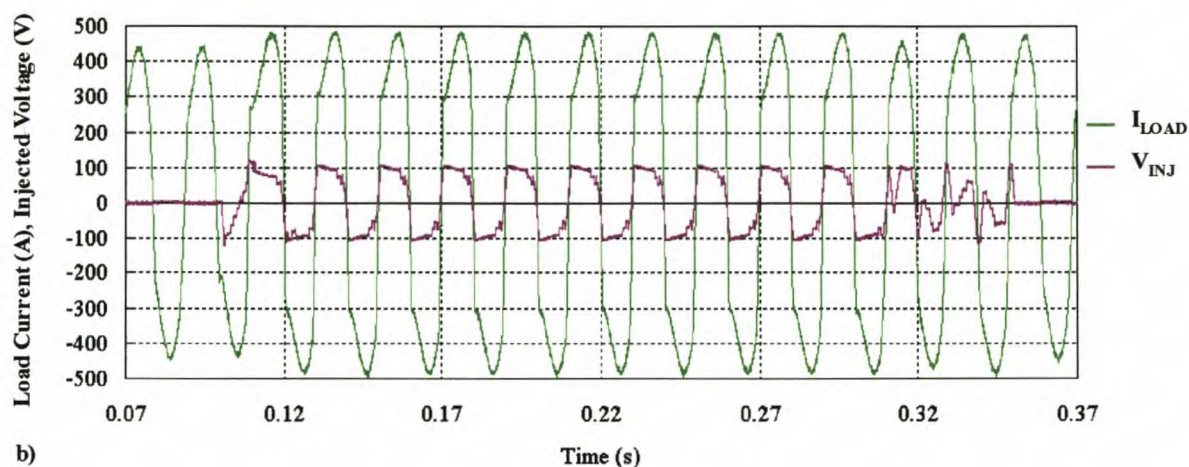
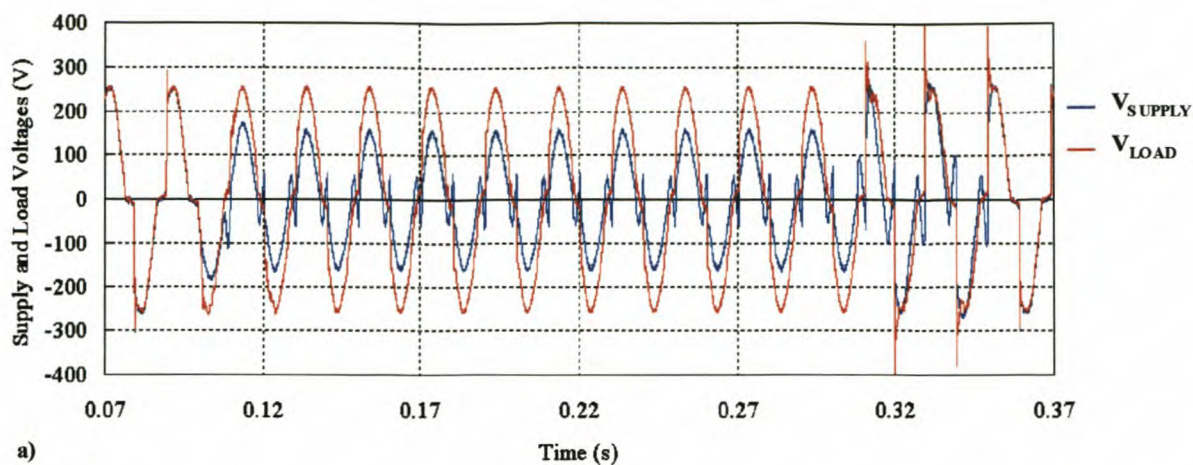


Figure 6.14: Dip compensation on a 38% dip for a non-linear load at 340 A_{RMS} : a) Load and supply voltages, b) Load current and injected voltage.

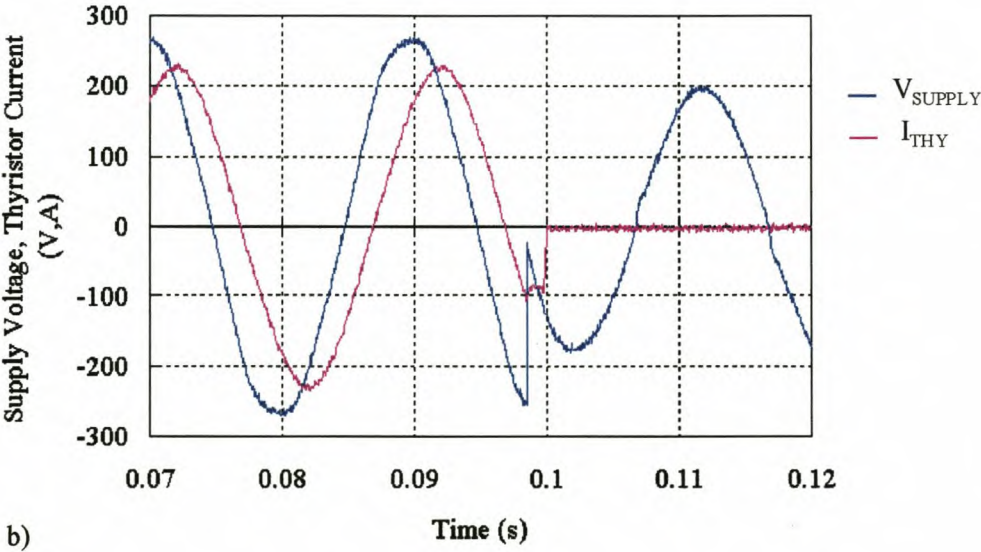
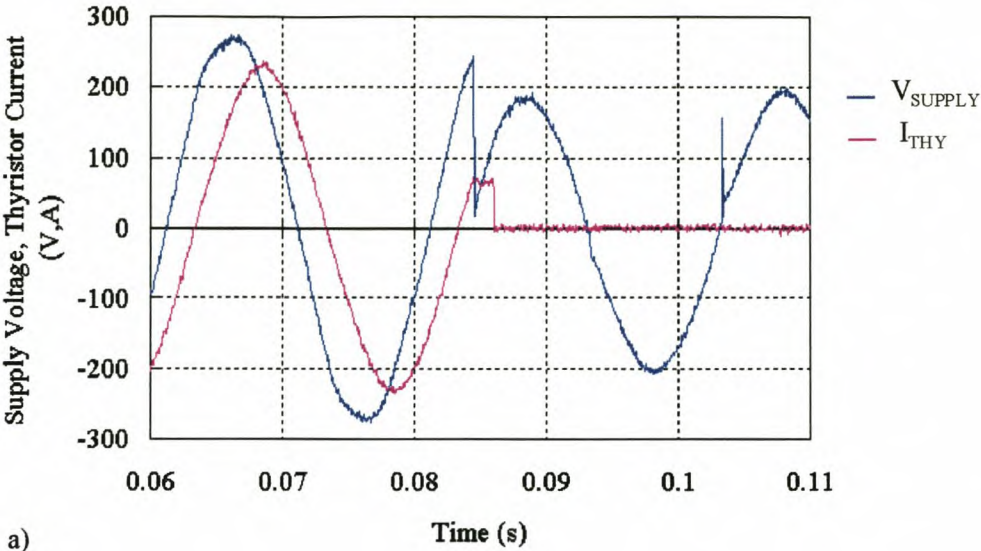
6.4 Verification of new control techniques

The new force commutation and power dissipation sharing techniques, described in paragraphs 5.6 and 5.7 and simulated in paragraph 5.8.1, were also verified in the practical results.

6.4.1 Force commutation

Dip compensation on a dip at a 28% depth with an inductive load at a 160 A_{RMS} load current was implemented to verify the force commutation method. Figure 6.15 shows the force commutation results for the four possible types of states of the supply voltage and load current. These results are similar to the simulations in Figure 5.35 - Figure 5.38. The results in Figure 6.15a and b show that

the thyristor current comes to an abrupt end shortly after the start of the dip, when the dip is detected, as expected. It seems that the thyristors take longer to commute when the polarities of the voltage and current differ (Figure 6.15 c and d), though this is not the case. It was verified that the control algorithm takes longer to detect the dip in the vicinity of these states, but the thyristors still commute immediately. The reason for this phenomenon is unknown.



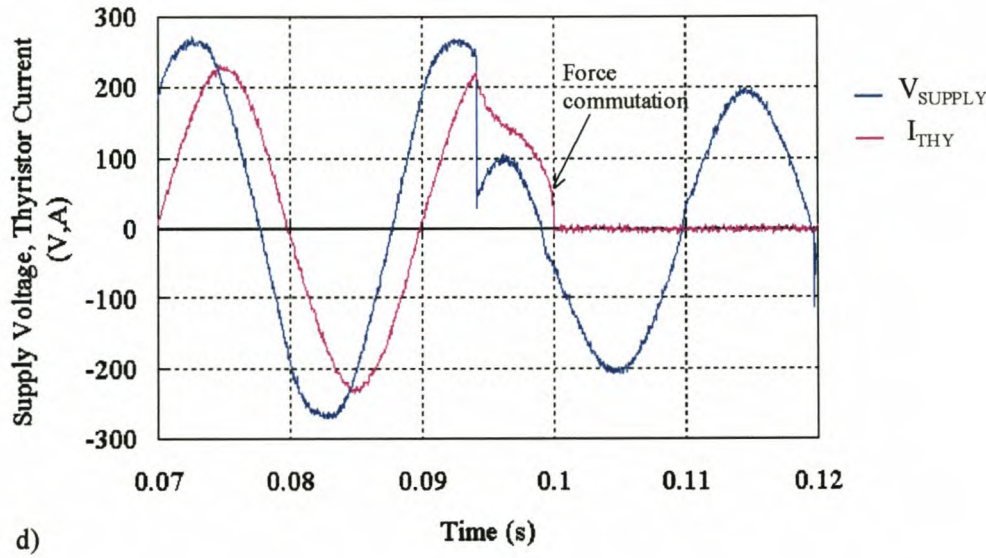
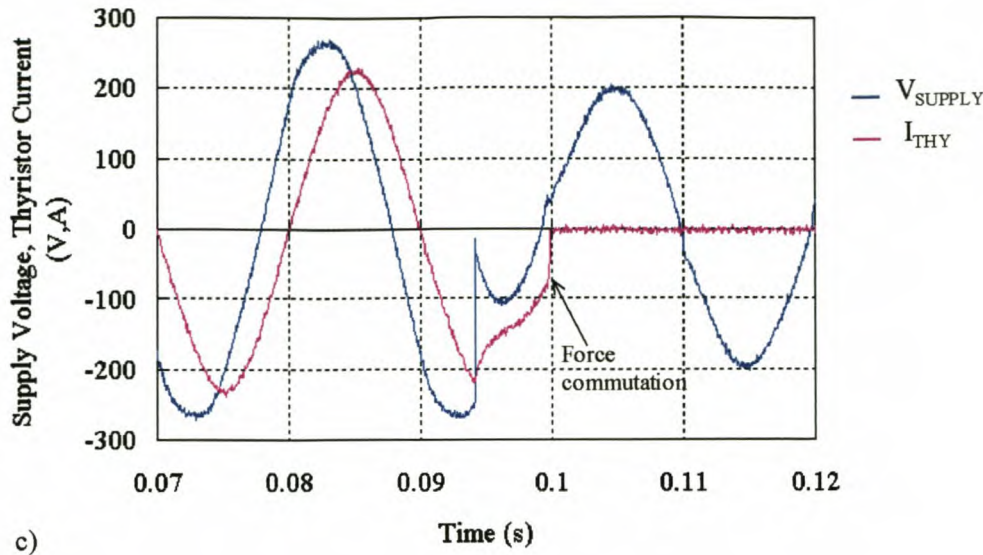
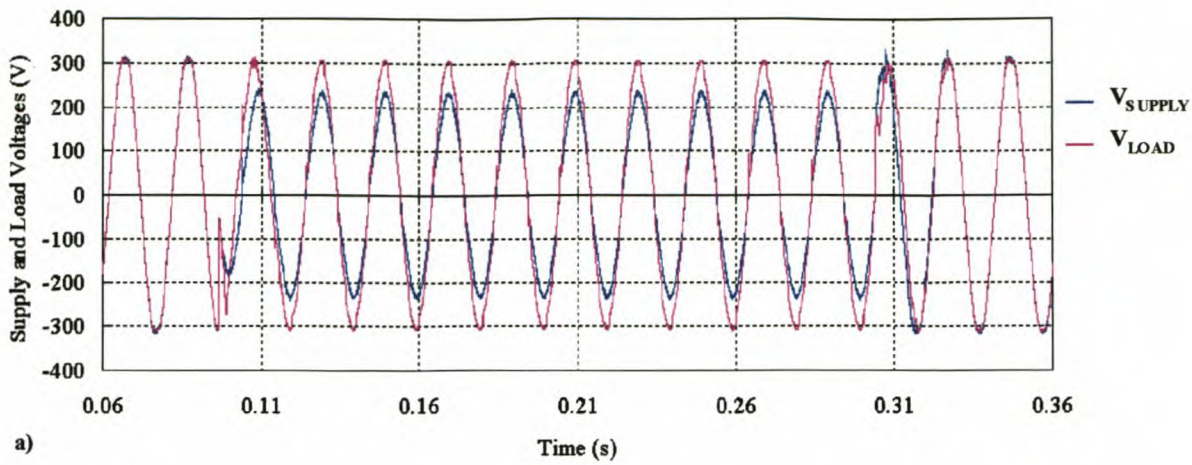


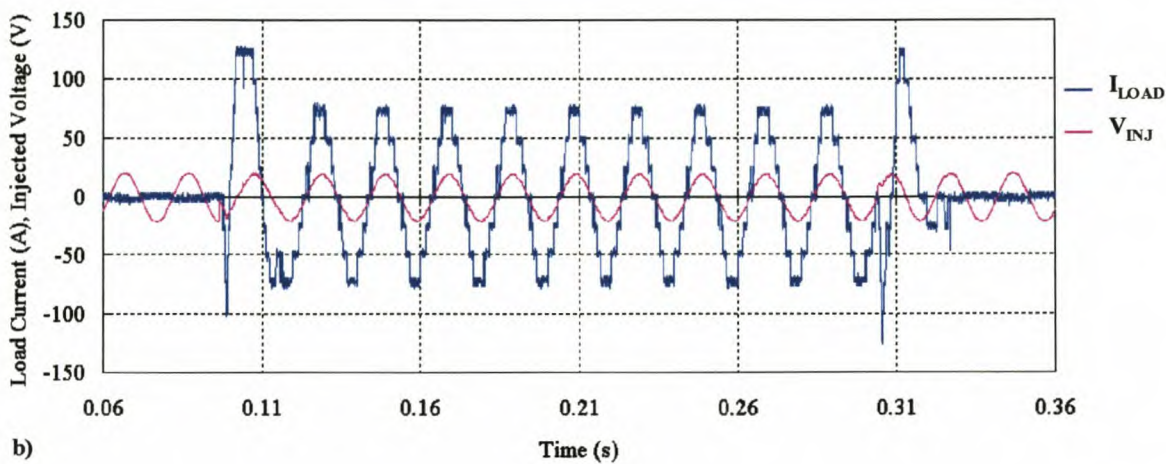
Figure 6.15: Force commutation with an inductive load: a) $V_{\text{SUPPLY}} > 0$ and $I_{\text{THY}} > 0$, b) $V_{\text{SUPPLY}} < 0$ and $I_{\text{THY}} < 0$, c) $V_{\text{SUPPLY}} > 0$ and $I_{\text{THY}} < 0$, d) $V_{\text{SUPPLY}} < 0$ and $I_{\text{THY}} > 0$.

6.4.2 Sharing of the power dissipation

A dip with a 24% depth and duration of 207 ms for a resistive load at a low current of 14.7 A_{RMS} was implemented to verify the new power dissipation sharing technique. This type of dip with its compensation is shown in Figure 6.16. Figure 6.16b shows that only three of the five inverters deliver a voltage step in each half cycle in the steady-state part of the dip. The sharing measurements were taken at this low current, because there was not enough high-current measuring equipment available that could measure the five DC bus currents simultaneously.



a)



b)

Figure 6.16: Dip compensation on a 24% dip for a resistive load at $14.7 A_{RMS}$: a) Load and supply voltages, b) Load current and injected voltage.

Figure 6.17 shows the integrated values of the square of each DC bus current for the duration of the type of dip in Figure 6.16. This result verifies the control method for the overall sharing of the power dissipation in all the batteries on the DC buses, although every inverter does not deliver current in each half cycle.

The sharing of the power dissipation in the switching components was also successfully verified. This measurement was implemented by measuring the gate signals of one inverter in synchronism with the load current. The square of the load current was then integrated for the on-state times of each switching component.

This part of the control was modified at first according to the conventional methods, where the switching components are switched according to a fixed switching pattern. Figure 6.18 shows the result for the conventional method with the fixed switching pattern. This result shows a large

difference in the total power dissipation between the top two and bottom two switches from time = 0.16 s onwards.

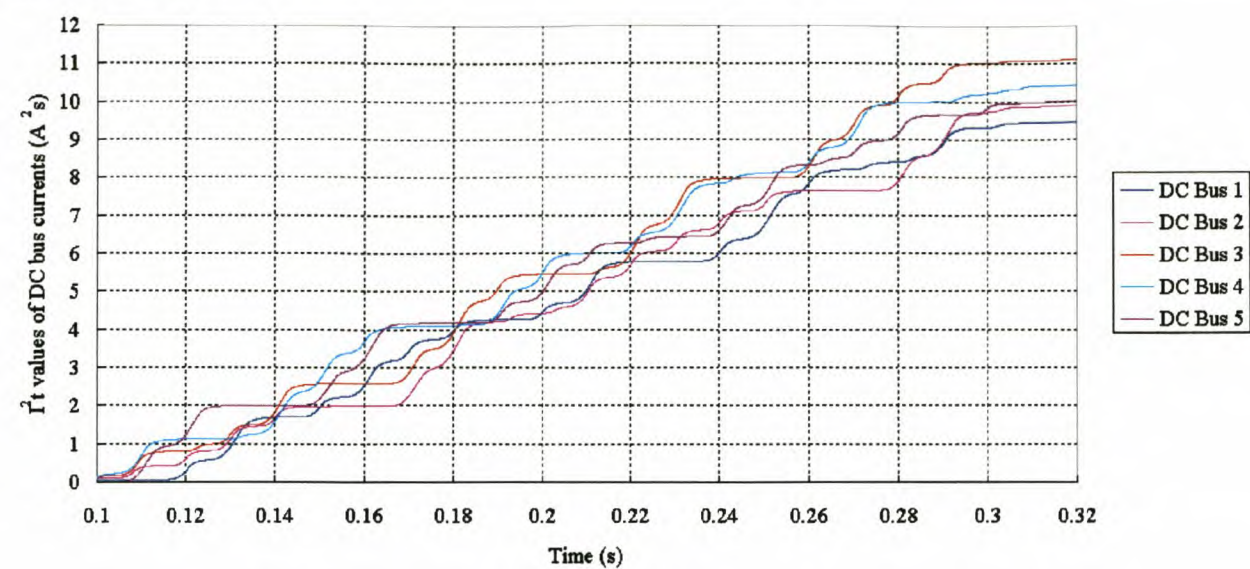


Figure 6.17: Estimation of the integrated power delivered by the DC buses.

The result with the new sharing method (Figure 6.19), on the other hand, shows an overall simultaneous increase in the total power dissipation in all four switches of one inverter. This result was taken in the same way as the one in Figure 6.18 for the same inverter.

The results in Figure 6.17 and Figure 6.19 prove that the sharing of the power dissipation in the MOSFETs and the batteries can be simultaneously implemented for series dip compensation with a multilevel inverter.

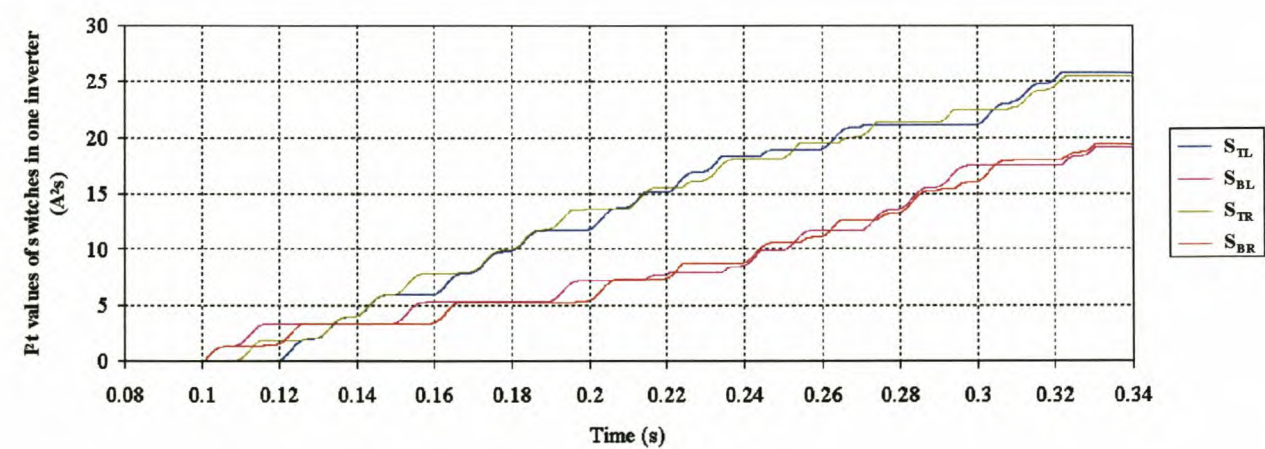


Figure 6.18: Estimation of the integrated power dissipated in all the switches of one inverter by using a fixed switching pattern.

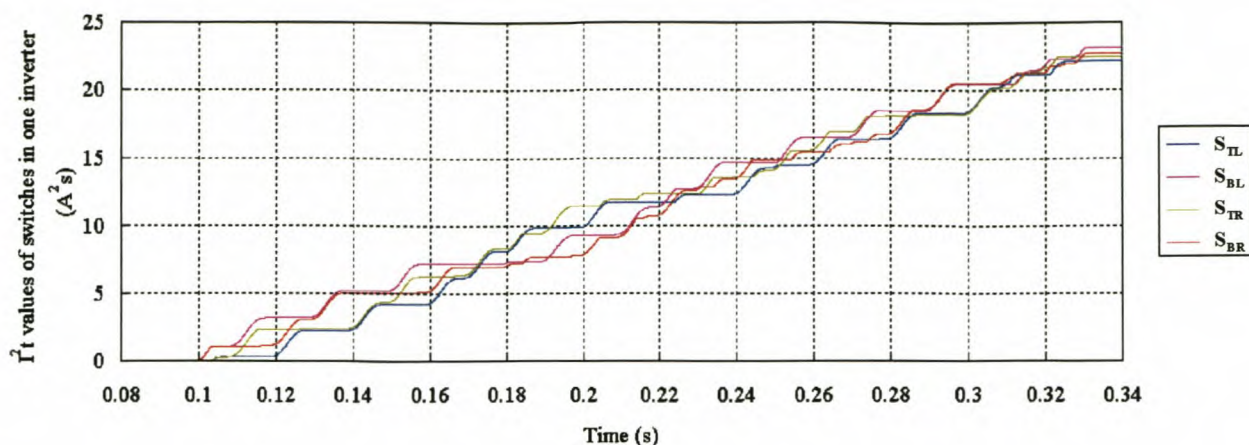


Figure 6.19: *Estimation of the integrated power dissipated in all the switches of one inverter by using the new method in this thesis.*

Summary

This chapter discussed the practical results on the single inverter and the multilevel inverter for series dip compensation.

The results on the single inverter proved that the low-cost UPS batteries could deliver the needed load current with a slight decrease in the battery voltage that is caused by the internal resistance. It also proved the capability of the automotive MOSFETs in parallel to conduct these currents and that the stray inductances would not cause a too large voltage overshoot across the MOSFETs at turn-off.

The dip compensation results proved to be successful and correlated with the simulations in the previous chapter. The only difference is the slightly smaller voltage steps, caused by the non-ideal properties of the batteries and the MOSFETs, but these were expected.

Finally, the new control methods for the force commutation and sharing of the power dissipation were also successfully verified.

7. Conclusion

The aim of this thesis was to develop a cost-effective dip compensator by eliminating the transformer and filter components that are usually present. A quick background on voltage dips and the present available solutions was given in the introduction. It showed that dips are the major power-quality concern for industries and also that most existing compensators do not justify the financial losses they compensate for.

A more thorough background on voltage dips followed in Chapter 2. It was shown that they are mainly caused by line electrical faults and that this is an increasing concern for the industry, because modern technical equipment is becoming more sensitive to voltage dips. The effects are large financial losses, usually because the process shutdowns, caused by voltage dips, result in lost production time and damaged products. A lot of measures already exist to compensate for this problem; they can be divided into two main groups, namely utility and customer solutions. Customer solutions in the form of power-conditioning equipment seem to be the most effective way to eliminate dips. A lot of power electronic converter technologies (UPS, active filters, AC-AC converters) have been developed for effective dip compensation, but they are very expensive. Transformers are the main contributors to these systems' cost. The advantage of series dip compensators is that the power rating of these systems can be reduced to compensate for dips up to a specified depth.

The possibilities of series dip compensation without a transformer were discussed and compared in Chapter 3. A new range of inverters, called multilevel inverters, was also discussed. The multilevel cascaded inverter topology was chosen as the most suitable multilevel inverter for transformerless series dip compensation. This topology eliminates extra clamping diodes and voltage balancing capacitors, which are present in the other topologies. This topology was compared with the single transformerless series inverter for cost-effectiveness. The multilevel cascaded inverter eliminates the output filter, it has lower switching losses than the single inverter and it is modular. This inverter was therefore chosen as a cost-effective topology for transformerless series dip compensation.

Chapter 4 discussed the hardware design of the proposed series dip compensator according to specifications for a small industrial load. Battery energy storage and paralleled automotive MOSFETs as switching components proved to be the most cost-effective components for the specified ratings. The MOSFET driver circuits and the design of the DC bus of the individual inverters were unique. Paralleled MOSFETs in the former and the low voltage and high current ratings in the latter made this a challenging design. The bus bars were also designed to withstand

fault currents for a short time duration and served as heatsinks to the MOSFETs, which have low switching losses. A pair of anti-parallel thyristors were added in parallel with the multilevel inverter in order to conduct the line current for normal and fault current conditions (fault currents are up to twenty times the rated current). The basic digital control was implemented with an established DSP control board.

The control methods of the multilevel inverter for series dip compensation were discussed in Chapter 5. Existing control techniques were evaluated to obtain the best possible techniques for dip detection and synchronisation for single-phase dip compensation. The way in which voltage steps are added to the supply voltage is also based on existing techniques. The existing techniques are based on the assumption of a relative steady-state output voltage, which is not the case for the transient nature of voltage dips. Because of this, a new technique for the sharing of the power dissipation in the switches and the batteries had to be developed. Finally, the control of the thyristors in the initiation and termination of dip compensation and the fault current protection was discussed. A new method for force commutation of the thyristors was also developed. Most of the control methods were confirmed with simulations in Simplorer.

Chapter 6 showed the practical results on the single inverter and the multilevel inverter for series dip compensation. The results on the single inverter proved the capability of the automotive MOSFETs in parallel to conduct the currents and that the stray inductances would not cause a too large voltage overshoot across the MOSFETs at turn-off. The dip compensation results proved to be successful and correlated with the simulations in the previous chapter. The only difference is the slightly smaller voltage steps, caused by the non-ideal properties of the batteries and the MOSFETs, but these were expected. Confirmation of the new control methods for the force commutation and sharing of the power delivery and power dissipation was also included.

The objectives (see Introduction) of this project were reached, and the following conclusions are drawn:

- The multilevel cascaded inverter topology proved to be the most cost-effective multilevel topology for transformerless dip compensation, because it has no extra clamping diodes and voltage-balancing capacitors;
- Batteries were chosen as the most cost-effective energy storage for this application's specifications;
- Control algorithms for the multilevel inverter for transformerless series dip compensation were developed, including two new techniques;
- A protection strategy for transformerless series injection devices was developed;
- A single-phase laboratory prototype of a 250 kVA transformerless dip compensator was designed and implemented and showed very good results.

7.1 Thesis contribution

The main contributions of this thesis are:

- A cost-effective, modular, transformerless series dip compensator that can easily be adapted for dips of larger depths by adding more inverter modules. This compensator was also patented;
- A comparison of the cost effectiveness of the energy-storage components for the inverter modules;
- A protection strategy for series compensators, together with a new force commutation technique was developed and implemented;
- A new control algorithm that implements the sharing of the power dissipation in the switching components and the batteries simultaneously was developed and implemented.

7.2 Future work

The main focuses of future work that can follow from this thesis are as follows:

a) Hardware:

- The inclusion of automatic battery chargers for each individual inverter.
- Upgrading of this compensator to a three-phase dip compensator. This will increase the power rating per phase for this dip compensator, because the phase shift must also be compensated for.

b) Control:

- Changing of the existing control algorithm to implement three-phase dip compensation. This will bring a change in the dip detection and synchronising techniques. It was stated in Chapter 5 that a better dip detection technique exists for three-phase dip compensation. The synchronising technique should also be upgraded to adapt to frequency drift and it must retain the original phase during a dip, because it cannot adapt gradually to the phase jump in a dip as in the case of single-phase dip compensation for single-phase loads;
- Improving the reliability of the system through a bypass algorithm [C-15] that will switch an individual inverter in the zero state if one of its switching components fails. An extra inverter module can also be included to improve the system's reliability.

c) Cost effectiveness:

The total component cost for the three-phase equivalent of this dip compensator was calculated and is shown in Table 7.1. It is assumed that an industrialised version of this compensator with added labour costs and a profit will result in a commercial price of about three times the total component cost (about R280 000). This price, for a 250 kVA load, will be just more than a R1 000/kVA. The aim is to build a dip compensator that will cost less than a R1 000/kVA.

Table 7.1: *Total component cost for the three-phase equivalent of this dip compensator.*

| Components | Cost [R] |
|---|------------|
| Batteries | 10 650.00 |
| Battery fuses | 2 490.00 |
| Bus capacitors | 3 030.00 |
| MOSFETs | 7 180.00 |
| Thyristors | 9 000.00 |
| Thyristor heatsinks | 500.00 |
| Copper for bus bars | 14 000.00 |
| PC boards | 30 900.00 |
| Optic fiber components | 9 050.00 |
| Digital controller and measuring equipment | 4 000.00 |
| Other electronic components (approximately) | 3 000.00 |
| Total component cost: | R93 800.00 |

Table 7.1 shows that the PC board layouts and the copper for the bus bars are the biggest single contributors to this system’s cost. In this project large and expensive PC board layouts were used. The temperature change calculations for fault currents in the bus bars also showed a very small temperature rise ($\Delta T = 2.94\text{ }^{\circ}\text{C}$).

For this project, the challenges for a cost-effective series dip compensator are therefore:

- A cost-effective bus bar design by reducing the amount of copper;
- Cost-effective PC board layouts by using smaller and cheaper layouts.

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Appendix A: Data on dips in South Africa

A.1 Extracts from NRS 048-2

Compatibility levels for voltage dips

NOTE — It is expected for most of the time and for most customers that the number of dips will be considerably less than the compatibility numbers set as the minimum standard. Indicative target values are given in NRS 048-4. The target values are provided in annex B for information only.

Table A.1: *Limits for the number of voltage dips per year for each category of dip window*

| 1 | 2 | 3 | 4 | 5 | 6 |
|--|---------------------------------|----|----|-----|-------------------|
| Network voltage range (see note 1) | Number of voltage dips per year | | | | |
| | Dip window category | | | | |
| | Z | T | S | X | Y (see note 2) |
| 6,6 kV to ≤ 44 kV | 20 | 30 | 30 | 100 | 150 |
| 6,6 kV to ≤ 44 kV rural | 49 | 54 | 69 | 215 | 314 |
| > 44 kV to ≤ 132 kV | 16 | 25 | 25 | 80 | 120 |
| 220 kV to ≤ 765 kV | 5 | 6 | 11 | 45 | 88 |
| NOTES | | | | | |
| 1 The network voltage is not necessarily the voltage at which the customer takes supply. It may be the voltage of the network that feeds the point of common coupling. Therefore, the set of Z, T, S, X and Y values applicable to a customer should be evaluated in each case, taking account of the network configuration supplying that customer. | | | | | |
| 2 The number of “Y” dips is provided for completeness of information, but it is not intended to regulate utilities on the basis of the number of “Y” dips. | | | | | |

Indicative targets for the number of voltage dips per year

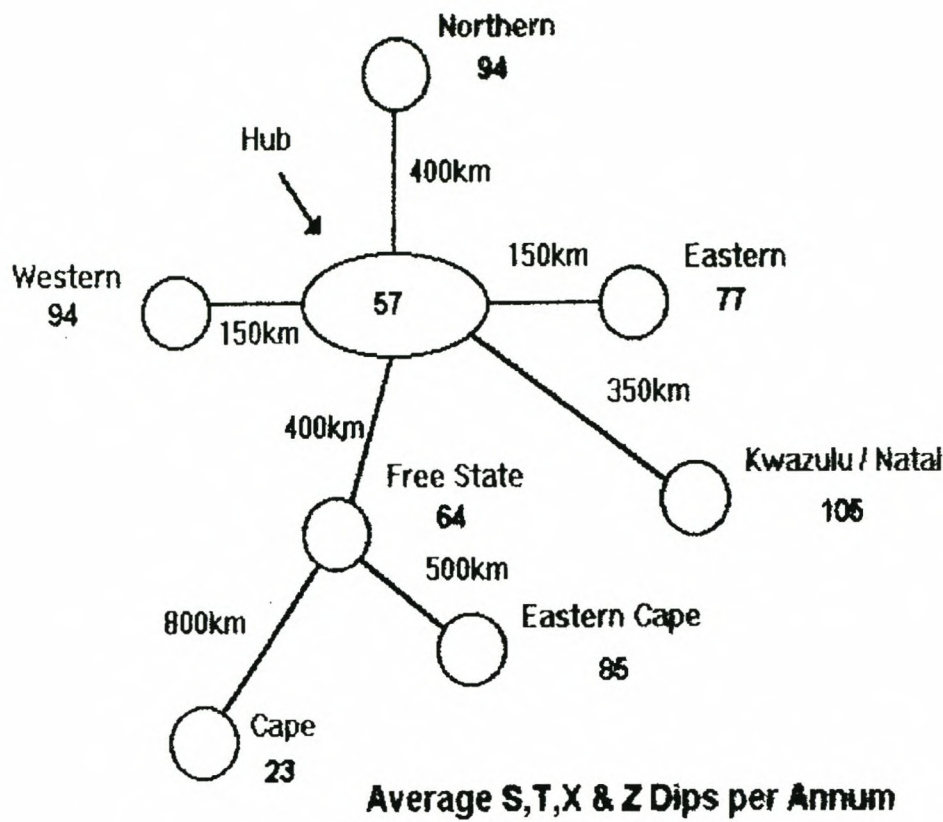
Table A.2: *Indicative targets for the number of voltage dips per year
for each category of dip window*

| 1 | 2 | 3 | 4 | 5 | 6 |
|-------------------------------------|---------------------------------|----|----|-----|-----|
| Network voltage range (see note) | Number of voltage dips per year | | | | |
| | Dip window category | | | | |
| | Z | T | S | X | Y |
| 6,6 kV to ≤ 44 kV | 10 | 8 | 10 | 50 | 75 |
| 6,6 kV to ≤ 44 kV rural | 20 | 15 | 25 | 100 | 150 |
| > 44 kV to ≤ 132 kV | 5 | 10 | 10 | 50 | 80 |
| 220 kV to ≤ 765 kV | 2 | 3 | 3 | 33 | 59 |

NOTE — The network voltage is not necessarily the voltage at which the customer takes supply. It may be the voltage of the network that feeds the point of common coupling. Therefore, the set of Z, T, S, X and Y values applicable to a customer should be evaluated in each case, taking account of the network configuration supplying that customer.

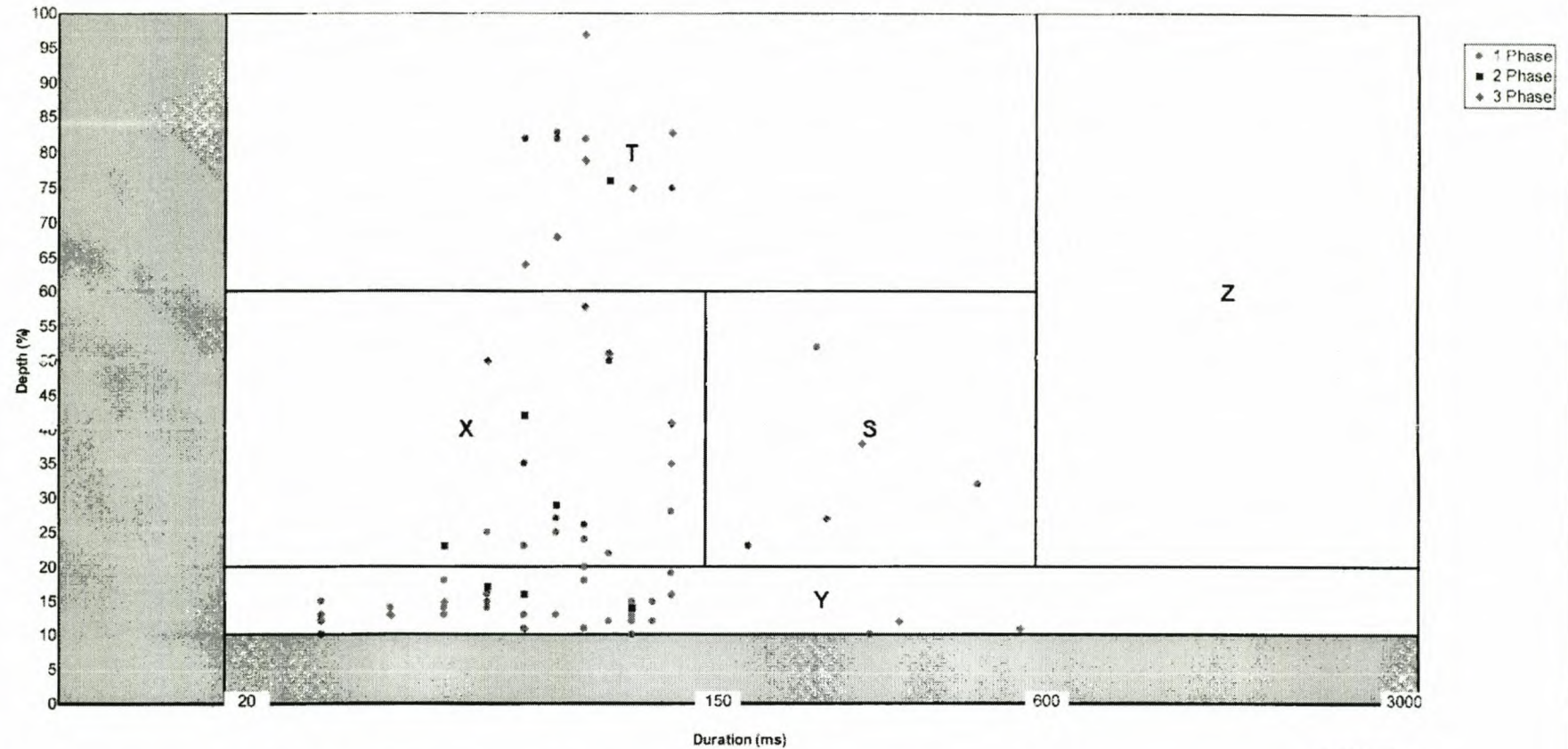
A.2 Transmission network data

DIPS IN SOUTH AFRICA



| Region | S Class | T Class | X Class | Z - Class |
|------------------|---------|---------|---------|-----------|
| Gauteng | 12-16 | 3-6 | 30-40 | 4 |
| Kwa-Zulu / Natal | 4-16 | 6-13 | 80-85 | 1-5 |
| W - Cape | 0-2 | 1-3 | 17-19 | 1-3 |
| E - Cape | 5 | 8 | 70 | 2 |
| FS&N - Cape | 5-12 | 6-18 | 30-50 | 2-10 |
| Mpumalanga | 10-18 | 6-10 | 40-55 | 5-7 |
| N & NW | 11-17 | 5-8 | 50-80 | 3-6 |

Scatter Plot for Stikland 132/66kV from 01/01/1999 to 31/12/1999



| Class | S | T | X | Y | Z |
|--------------|---|----|----|----|---|
| Single Phase | 3 | 5 | 13 | 37 | 0 |
| Two Phase | 0 | 1 | 3 | 3 | 0 |
| Three Phase | 2 | 7 | 5 | 6 | 0 |
| Total | 5 | 13 | 21 | 46 | 0 |

Valid Days: 334
Total Days: 365

All Dips Selected

Auxiliary Outages

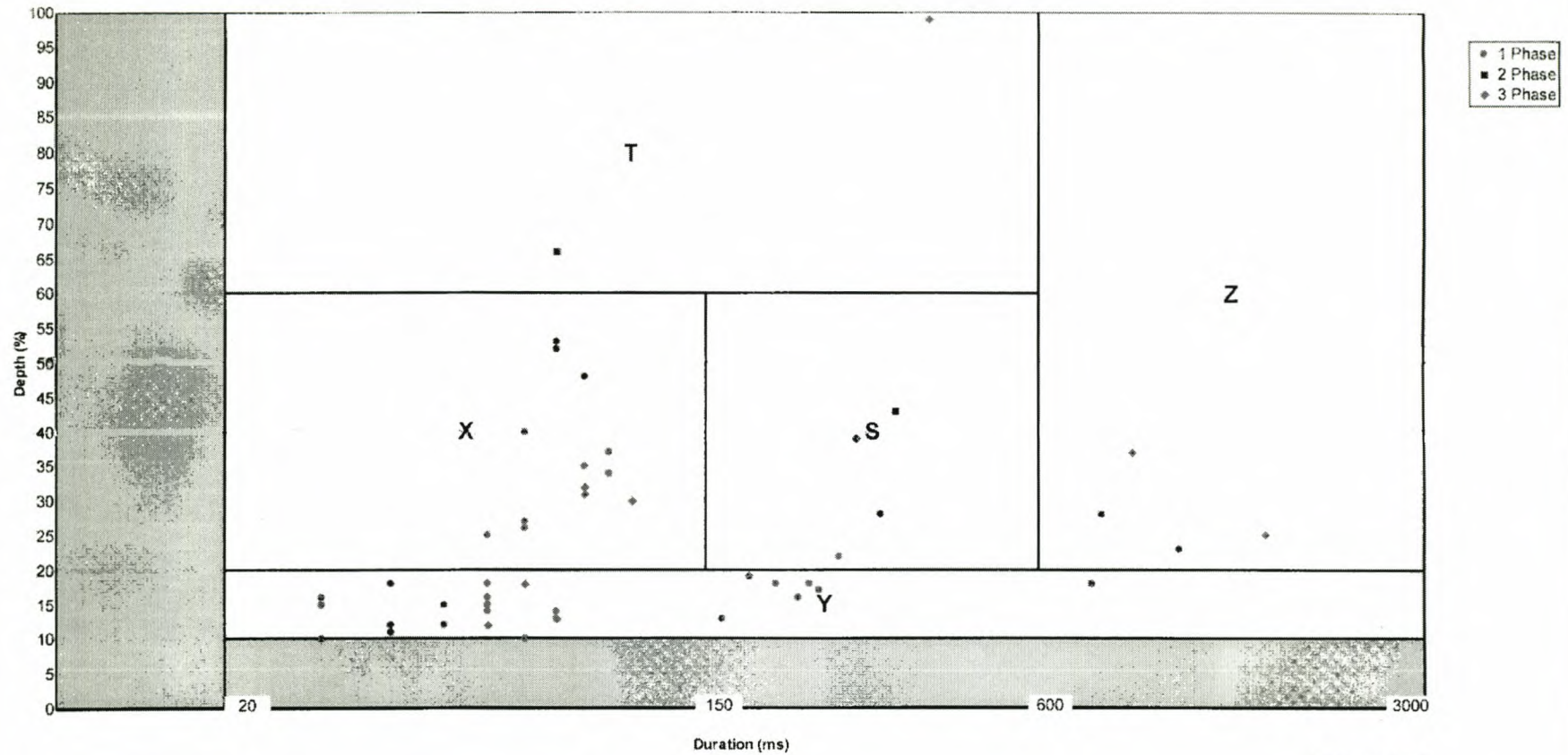
| Start Date | End Date |
|------------------------|------------------------|
| 18/01/1999 06:23:42 PM | 18/01/1999 06:37:08 PM |
| 22/02/1999 07:24:16 AM | 22/02/1999 10:44:00 AM |

Scatter Plot for Stikland 132/66kV from 01/01/1999 to 31/12/1999

1

24/03/2000

Scatter Plot for Jupiter 275/88kV from 01/01/1999 to 31/12/1999



| Class | S | T | X | Y | Z |
|--------------|---|---|----|----|---|
| Single Phase | 2 | 0 | 10 | 26 | 3 |
| Two Phase | 1 | 1 | 0 | 0 | 0 |
| Three Phase | 1 | 1 | 3 | 3 | 1 |
| Total | 4 | 2 | 13 | 29 | 4 |

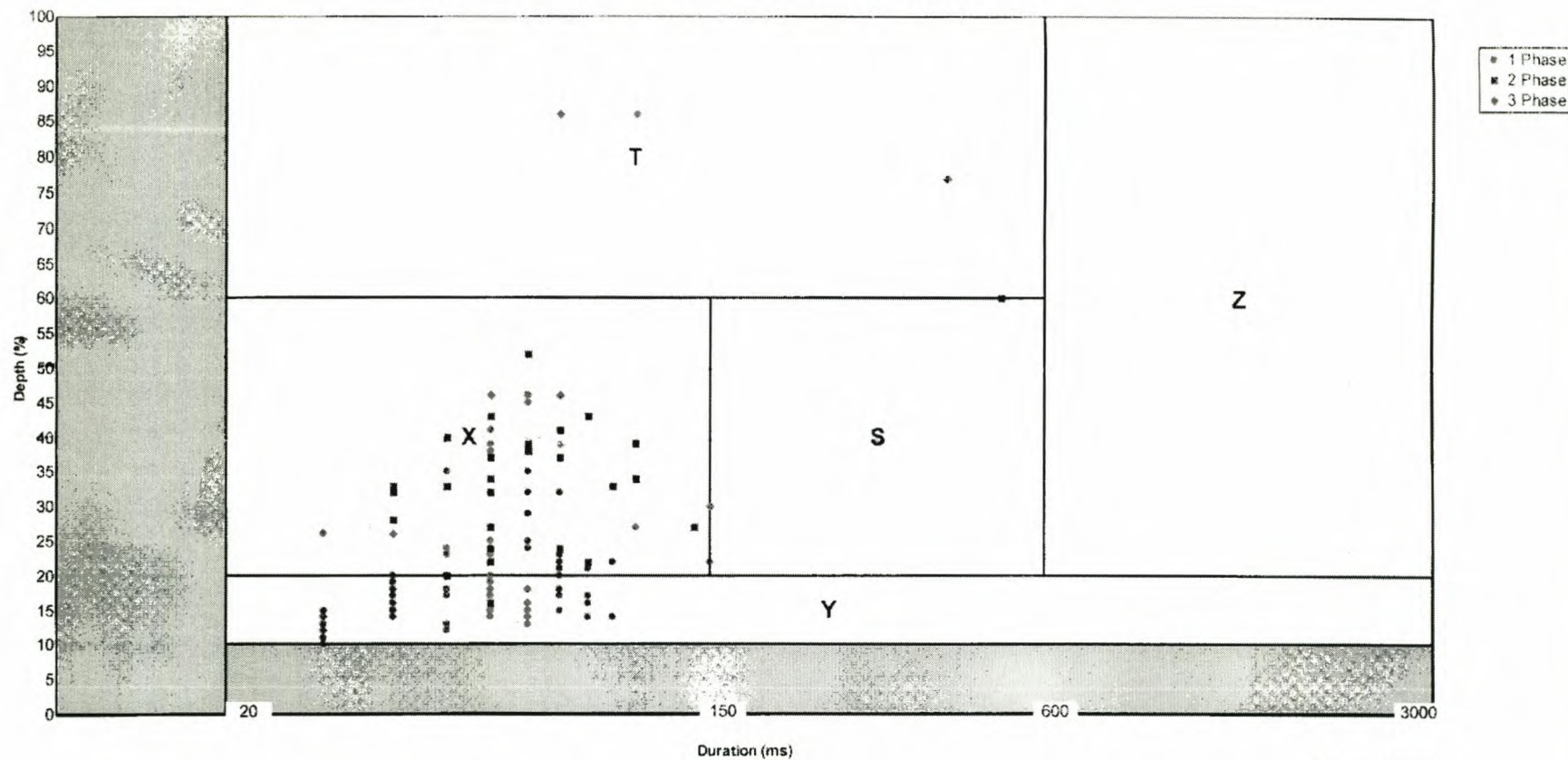
Valid Days: 340
Total Days: 365

All Dips Selected

Auxiliary Outages

Start Date End Date

Scatter Plot for Impala 275/132kV from 01/01/1999 to 31/12/1999



| Class | S | T | X | Y | Z |
|--------------|---|---|----|----|---|
| Single Phase | 0 | 0 | 37 | 59 | 0 |
| Two Phase | 0 | 1 | 28 | 1 | 0 |
| Three Phase | 0 | 3 | 5 | 0 | 0 |
| Total | 0 | 4 | 70 | 60 | 0 |

Valid Days: 364
Total Days: 365

All Dips Selected

Auxiliary Outages

Start Date End Date

Appendix B: Circuit diagrams

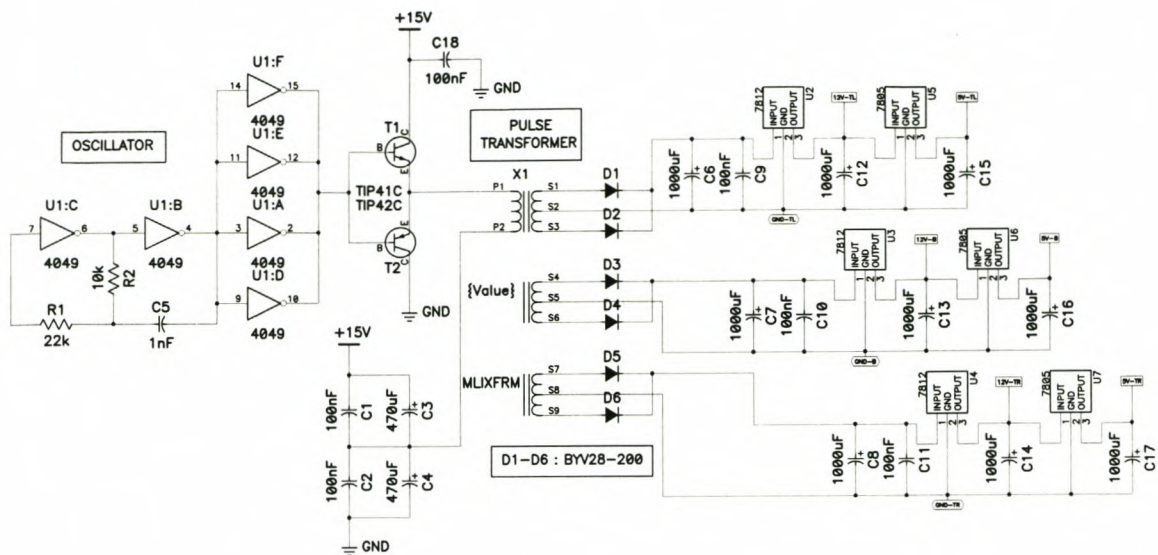


Figure B.1: *Isolated power supply for each inverter.*

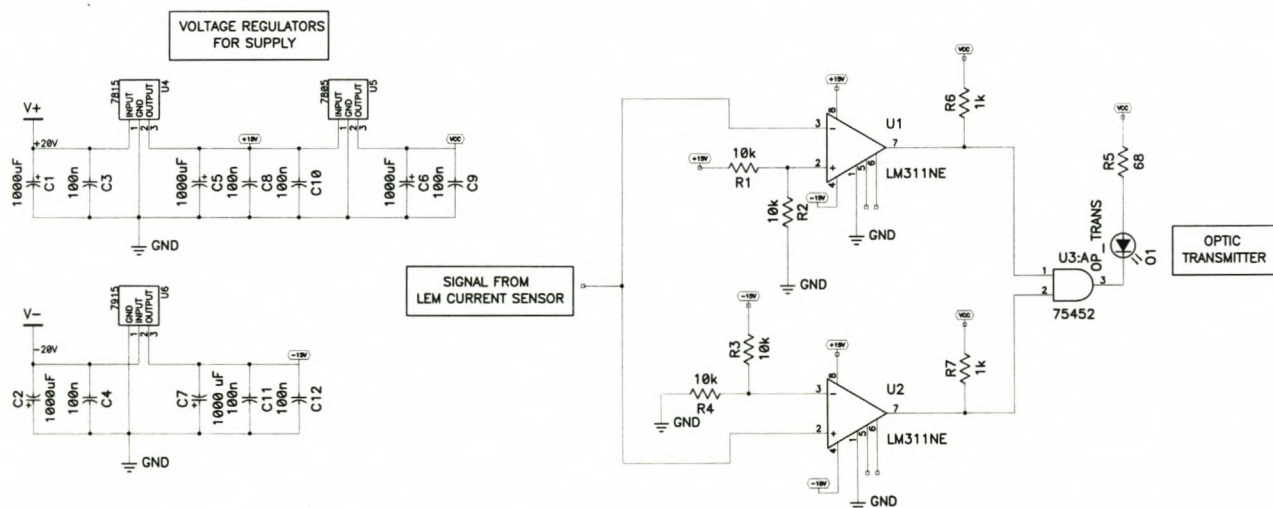


Figure B.2: *Fault current detection circuit.*

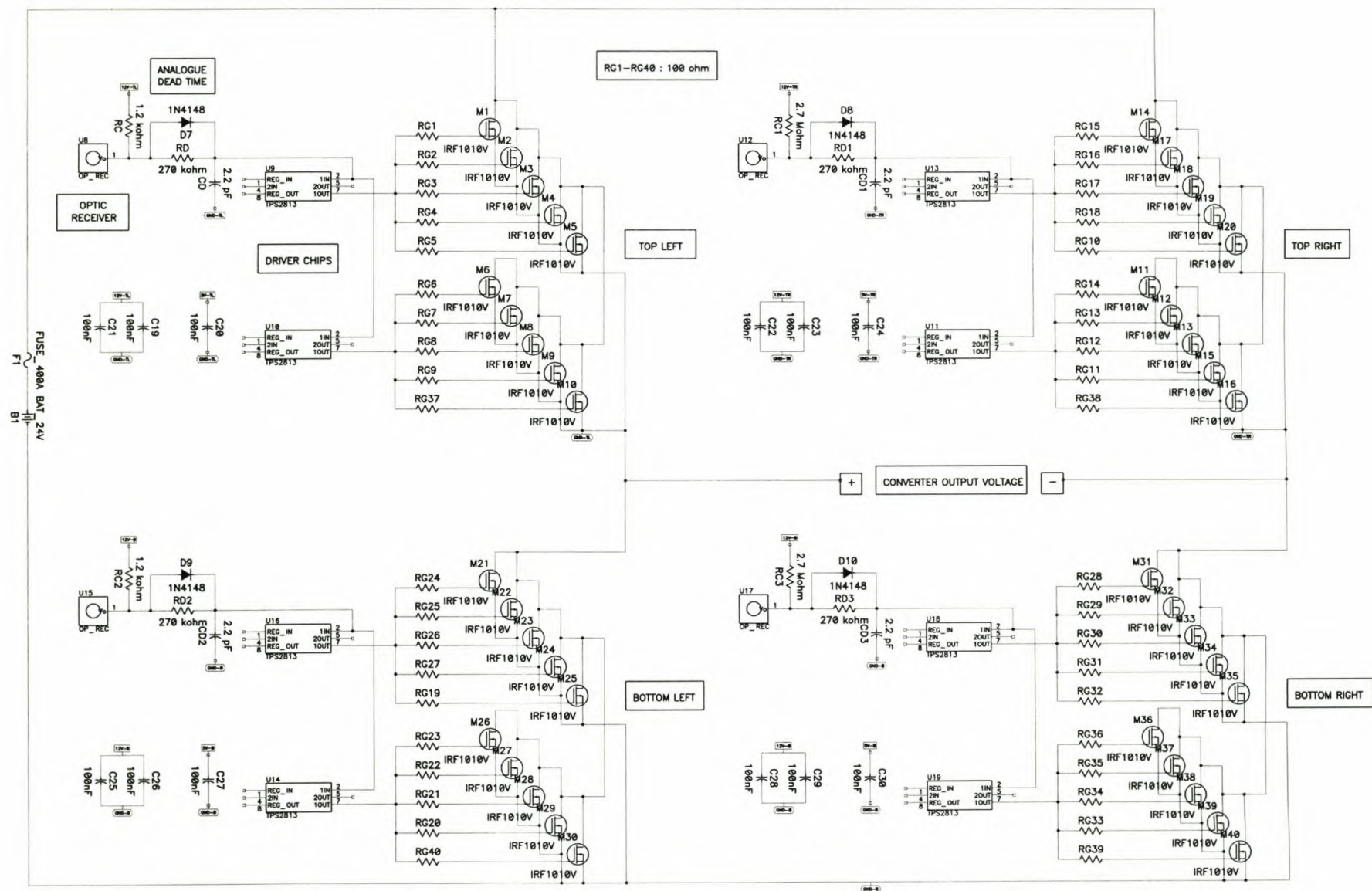


Figure B.3: Circuit diagram of each inverter, including the driver circuits and optic receivers for the optic fibres.

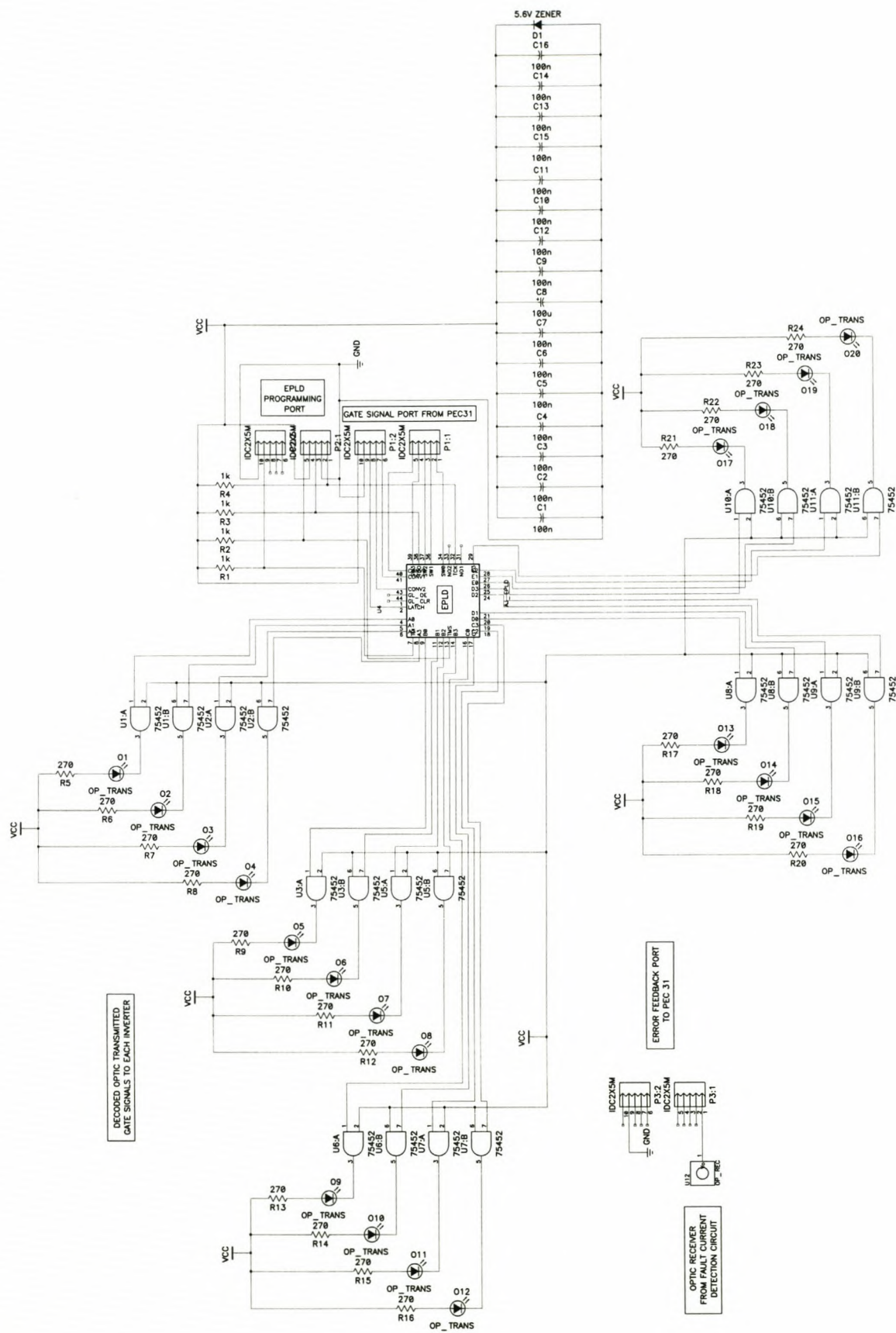


Figure B.4: Gate signal multiplexer circuit.

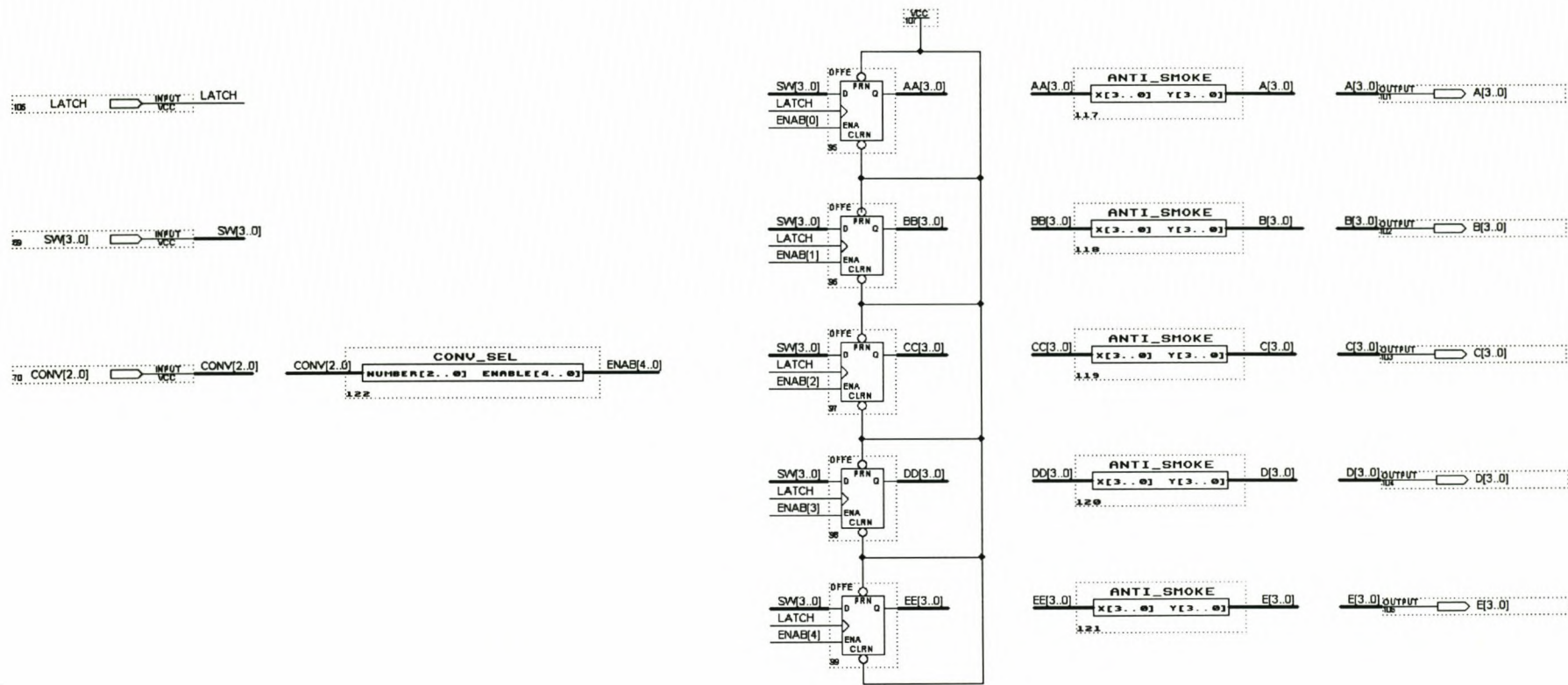


Figure B.5: Schematic diagram of the programmed gate signal multiplexer in the EPLD.

Appendix C: Matlab source code

Generation of the amplitude and reference signal with the $\frac{1}{4}$ cycle relationship for dip detection and synchronisation (Figure 5.6, Figure 5.7, Figure 5.10).

```
%-----%
% Matlab source code:                                qcycle.m                                %
% Author: A.J. Visser                                Date: 2000-03-10                                %
%                                                     %
% This code is the main simulation of the 1/4 cycle relationship for dip %
% detection and synchronization.                        %
%-----%

% Set parameters %
F = 50;          % Line frequency                    %
Fs = 5000;       % Sampling frequency                %
N1 = 500;        % Sampling points in simulation %
Nn = 100;
Nd = 300;

% Simulated dip with function 'sinus' %
f1 = [327*sinus(F,Fs,4.189,Nn)                229*sinus(F,Fs,3.665,Nd)
327*sinus(F,Fs,4.189,Nn)];

% Function 'qcr' implements dip detection and synchronization with the %
% 1/4 cycle relationship. %
[q,d,dq,dqavg,ref] = qcr(f1,F,Fs,N1);

% Plot of figure 5.6 %
figure(1);
subplot(2,1,1),plot ([0:N1-1]/Fs,f1); ylabel('a) Phase voltage [V]');
axis([0 0.1 -400 400]);
subplot(2,1,2),plot ([0:N1-1]/Fs,dq); ylabel('b) Value of A [V]');
xlabel('Time [sec]');
axis([0 0.1 0 400]);

% Plot of figure 5.7 %
figure(2);
hold on;
plot ([0:N1-1]/Fs,dqavg);
axis ([0 0.1 0 400]);
ylabel('Average value of A [V]');
xlabel ('Time [s]');

% Plot of figure 5.10 %
fx = 327*ref;
figure (3);
hold on;
plot ([0:N1-1]/Fs,f1,'b');
plot ([0:N1-1]/Fs,fx,'r');
ylabel('Supply voltage (thick) and Reference signal (thin) [V]');
xlabel('Time [s]');
hold off;
```

```

%-----%
% Matlab source code:                                qcr.m                                %
% Author: A.J. Visser                                Date: 2000-03-10                                %
%                                                     %
% This code is the 1/4 cycle relationship function that generates the values %
% of A and the average of A for dip detection and also the synchronization %
% signal for the simulation in qcycle.m %
%-----%

function [fq,fd,fdq,fdqavg,fref] = qcr(f,F,Fs,N);
% Parameter definitions %
% fq - Asin(...) %
% fd - Acos(...) %
% fdq - Value of A %
% fdqavg - Average of A %
% fref - Unit synchronized signal %
% f - Generated signal with dip %
% F - Line frequency %
% Fs - Sampling frequency %
% N - Sampling points in simulation %

% lg - sampling points in a 1/4 cycle %
lg = Fs/(4*F);

for n = 1:N;
    % Values after the first 1/2 cycle %
    if n >= 2*lg + 1;
        fq(n) = f(n-lg);
        fd(n) = f(n);
        fdq(n) = sqrt( (fq(n))^2 + (fd(n))^2 );
        fdqavg(n) = (sum(fdq(n-lg+1:n)))/lg;
        fref(n) = fd(n)/fdq(n);
    % Values after the first 1/4 cycle %
    elseif n >= lg+1;
        fq(n) = f(n-lg);
        fd(n) = f(n);
        fdq(n) = sqrt( (fq(n))^2 + (fd(n))^2 );
        fdqavg(n) = 327;
        fref(n) = fd(n)/fdq(n);
    % Values in the first 1/4 cycle %
    else;
        fq(n) = 0;
        fd(n) = 0;
        fdq(n) = 327;
        fdqavg(n) = 327;
        fref(n) = f(n)/327;
    end;
end;
end;

```


Generation of the reference signal with the correlation method for synchronisation
(Figure 5.11).

```

%------%
% Matlab source code:                                correlat.m          %
% Author: A.J. Visser                                Date: 1999-11-02                %
%                                                     %
% This code is the main simulation of the correlation method for          %
% synchronization.                                     %
%------%

% Set parameters %
F = 50;          % Line frequency                                %
Fs = 5000;       % Sampling frequency                            %
N1 = 800;        % Sampling points in simulation %
Nn = 200;
Nd = 400;

% Simulated dip with function 'sinus' %
f1 = [327*sinus(F, Fs, 4.189, Nn)          229*sinus(F, Fs, 3.665, Nd)
327*sinus(F, Fs, 4.189, Nn)];

% Function 'corr' implements dip detection with the 1/4 cycle relationship %
% and synchronization with the correlation method.                             %
[dq, ref] = corr(f1, Fs, N1, 327);

% Plot of figure 5.11 %
figure(1);
hold on;
axis([0 0.16 -400 400]);
plot([0:N1-1]/Fs, f1, 'b');
plot([0:N1-1]/Fs, ref, 'r');
ylabel('Supply voltage (thick) and Reference signal (thin) [V]');
xlabel('Time [sec]');
hold off;

```

```

%-----%
% Matlab source code: qcr.m %
% Author: A.J. Visser Date: 1999-05-11 %
% %
% This code is the correlation method's function that generates the %
% synchronizing signal for the simulation in qcycle.m, including the values %
% of A with the 1/4 cycle relationship for dip detection. %
%-----%

function [fdq,ref] = corr(f,Fs,N,amp);
% Parameter definitions %
% fdq - Value of A %
% ref - Synchronized signal %
% f - Generated signal with dip %
% Fs - Sampling frequency %
% N - Sampling points in simulation %
% amp - Amplitude of Voltage %

% M - Sampling points in a 1 cycle %
M = Fs/50;

% ks - Sampling points in a 1/4 cycle %
ks = M/4;

for n = 1:N;
    % Values after the first cycle %
    if n >= M;
        fd(n) = f(n);
        fq(n) = f(n-ks);
        fdq(n) = sqrt( (fq(n))^2 + (fd(n))^2 );
        for i = 1:M;
            Rfs(i) = sum(f(n-M+1:n).*sin(2*pi/M*([1:M]+i)));
        end;
        [y,i] = max(Rfs);
        ref(n) = amp*sin(2*pi*i/M);
    % Values after the first 1/4 cycle %
    elseif n >= ks+1;
        fd(n) = f(n);
        fq(n) = f(n-ks);
        fdq(n) = sqrt( (fq(n))^2 + (fd(n))^2 );
        ref(n) = f(n);
    % Values in the first 1/4 cycle %
    else;
        fq(n) = 0;
        fd(n) = 0;
        fdq(n) = 0;
        ref(n) = f(n);
    end;
end;

```


Generation of the amplitude and reference signal with the dft method for dip detection and synchronisation (Figure 5.4, Figure 5.12).

```
%-----%
% Matlab source code:                                dft_meth.m
% Author: A.J. Visser                                Date: 2000-03-13
%
% This code is the main simulation of the dft method for dip detection and
% synchronization.
%-----%

% Set parameters %
F = 50;          % Line frequency
Fs = 5000;       % Sampling frequency
N1 = 800;        % Sampling points in simulation
Nn = 200;
Nd = 400;

% Simulated dip with function 'sinus' %
f1 = [327*sinus(F,Fs,4.189,Nn) 229*sinus(F,Fs,3.665,Nd) 327*sinus(F,Fs,4.189,Nn)
];

% Function 'dftr' implements dip detection and synchronization with the %
% dft method.
[dq1,ref1] = dftr(f1,Fs,N1,327);

% Plot of figure 5.12 %
figure(1);
hold on;
axis([0 0.16 -400 400]);
plot([0:N1-1]/Fs,f1,'b');
plot([0:N1-1]/Fs,ref1,'r');
ylabel('Supply voltage (thick) and Reference signal (thin) [V]');
xlabel('Time [sec]');
hold off;

% Plot similar to figure 5.4 %
figure (2);
subplot(2,1,1),plot ([0:N1-1]/Fs,f1); ylabel('a) Phase voltage [V]');
axis([0 0.16 -400 400]);
subplot(2,1,2),plot ([0:N1-1]/Fs,dq1); ylabel('b) 50 Hz Amplitude [V]');
xlabel('Time [sec]');
axis([0 0.16 0 400]);
```

```

%-----%
% Matlab source code:                                dftr.m
% Author: A.J. Visser                                Date: 1999-10-08
%
% This code is the dft method's function that generates the values of the
% amplitude and reference signal for dip detection and synchronization in
% the simulation in dft_meth.m
%-----%

function [Sdq,ref] = dftr(f,Fs,N,amp);
% Parameter definitions
% Sdq - Value of the amplitude
% ref - Synchronized signal
% f - Generated signal with dip
% Fs - Sampling frequency
% N - Sampling points in simulation
% amp - Amplitude of Voltage

% Precalculated values of the sine and cosine waveforms %
i = 1:100;
sinus = sin(2*pi*i/100);
cosinus = cos(2*pi*i/100);

% Sampling points in one cycle %
M = Fs/50;

% Index for circular buffer %
afset = 1;

% Flag that signal the end of the first cycle's sampling points %
vlag = 0;

% ***** %
for n = 1:N;
    afset = afset + 1;
    if afset < M+1;
        siklus(afset-1)=f(n);
    else
        afset = 1;
        siklus(M) = f(n);
    end;

% Amplitude and reference signal are calculated after the first cycle %
    if vlag==1
        % SomRe and SomIm are the sums of the real and imaginery values %
        % for the calculation of the fundamental DFT component.
        SomRe = 0;
        SomIm = 0;
        indeks = afset;
        for m=1:M
            SomRe = SomRe + siklus(indeks)*cosinus(m);
            SomIm = SomIm + siklus(indeks)*sinus(m);
            indeks = indeks + 1;
            if indeks == 101
                indeks = 1;
            end;
        end;

        Sdq(n) = sqrt(SomRe*SomRe + SomIm*SomIm)*0.02;
        ref(n) = amp*(SomRe/(Sdq(n)*50));

% Values in the first cycle %
    else
        if (afset == 1)

```



```

        vlag = 1;
    end;
    Sdq(n) = 327;
    ref(n) = f(n);
end;

% End of the 'for' loop %
end;

```

The sinusoidal signal function, called 'sinus'.

```

%-----%
% Matlab source code:                sinus.m                %
% Author: A.J. Visser                Date: 2000-11-14 (updated) %
%                                     %                       %
% This code is the sinusoidal function that assist in the generation of the %
% supply siganl with a dip in the following simulations: qcycle.m, %
% correlat.m and dft_meth.m %
%-----%

function x = sinus(F,Fs,Q,N);
% Parameter definitions %
% x - Sinusoidal signal %
% F - Line frequency %
% Fs - Sampling frequency %
% Q - Phase %
% N - Number of sampling points %

% Sampling period %
Ts = 1/Fs;

n = 1:1:N;
x = sin(2*pi*F*n*Ts + Q);

```

Appendix D: Other practical results

It was stated in Chapter 6 that a scale model of this dip compensator was built to verify the control methods for dip compensation. The most important practical results are given in this Appendix. A quick overview on other results of the single inverter and the full-scale dip compensator is also included.

D.1 Scale model

An experimental laboratory scale model of this compensator, consisting of 5 inverters in series to compensate for dips of up to 30% in depth was built before the design of the full-scale model. This scale model was built to prove the concept and also to test and refine the control algorithm.

The scale model was tested at the rated voltage (230 V_{RMS} phase voltage) but at about 3.3%(12 A) of the rated current. The multilevel inverter was built up with half-bridge IGBT phase-arm modules, developed at the University of Stellenbosch for undergraduate practical work. These modules are rated at a bus voltage of 500V and a current of 15A with a bus capacitance of 1100 μ F. The multilevel inverter was tested with a 24 V bus on each inverter, which consists of two 12V UPS batteries (SOLAR 105) in series.

The same thyristors used in the results for the full-scale model were also used for the bypass and protection in the testing of the scale model.

The control, as described in Chapter 5, was implemented through the PEC31 DSP controller board, also developed at the University of Stellenbosch.

This compensator was tested for dips on different loads. All the important aspects of the control were also verified.

D.1.1 Verification of control concepts

A few results were taken to verify the control concepts that were discussed in the chapter on control.

a) Staircase sine waveform

A practical verification of the simulation in Figure 5.39 is shown in Figure D.1. This is the largest steady-state staircase sine waveform which can be injected in series with the line for dip compensation by the multilevel cascaded inverter described above. The staircase waveform was synchronised with a 50 Hz sine wave reference (also shown in Figure D.1). This result proves the staircase sine waveform concept.

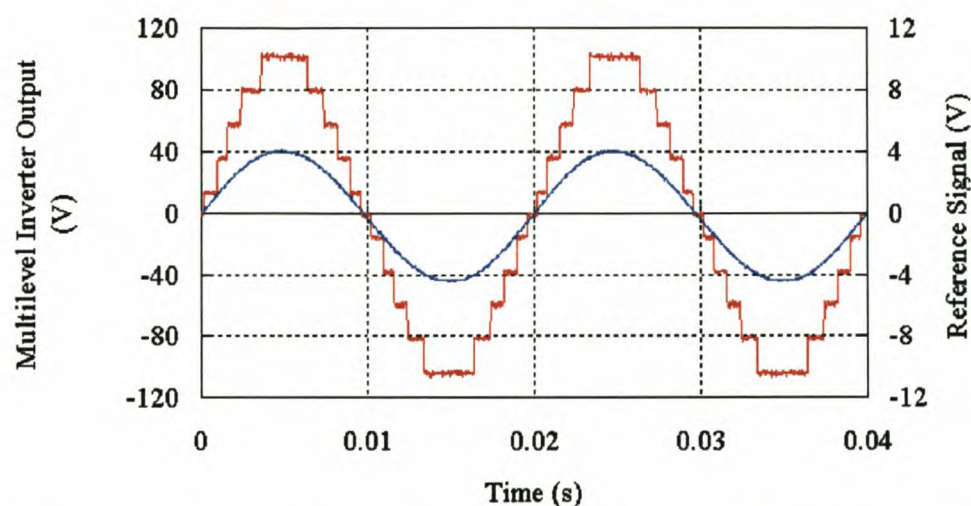


Figure D.1: Synchronised sine staircase waveform output of multilevel inverter with 5 inverters in cascade.

b) Force commutation

The chapter on control showed a special technique to force commute the anti-parallel thyristors at the start of the dip. This concept is verified here with results on three different types of loads. Figure D.2 and Figure D.3 show the force commutation at the beginning of a 15% dip on the resistive and non-linear loads. These two figures show the supply voltage and thyristor current at the time when the dip starts. The resistive load's value was 15.9Ω and the non-linear load consisted of a single-phase diode bridge with a 47 mH inductor and a 19.5Ω resistor in series at its output.

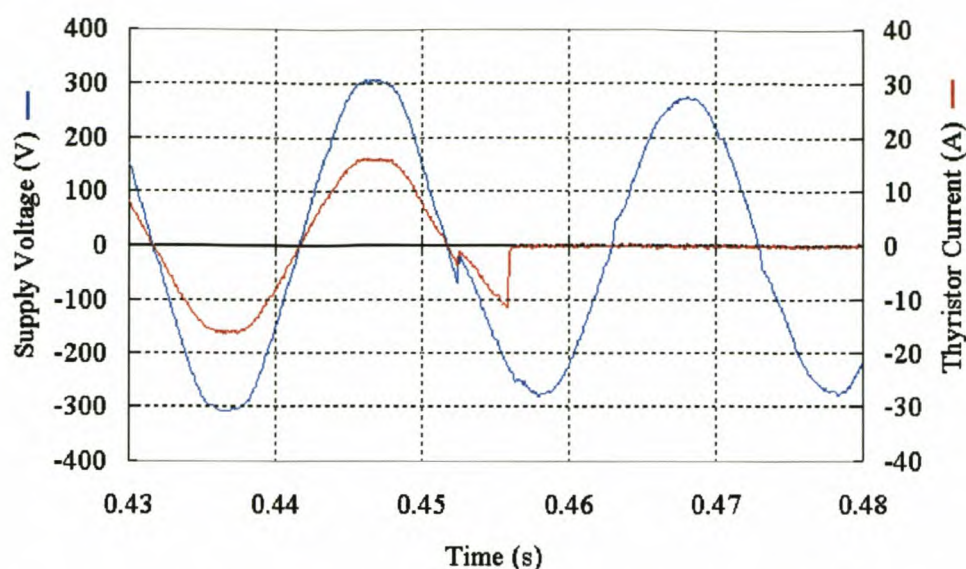


Figure D.2: Force commutation with a resistive load (15% dip)

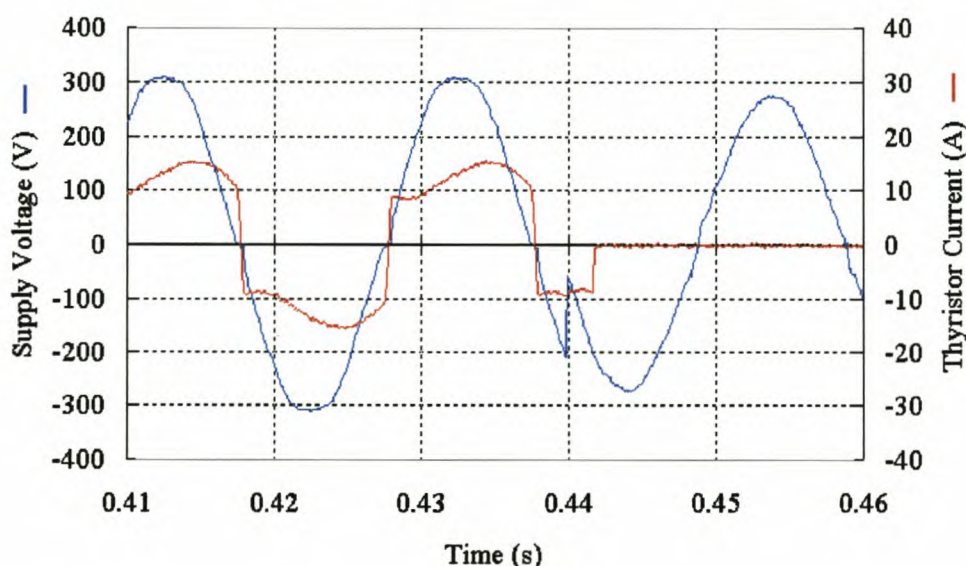


Figure D.3: Force commutation with a non-linear load (15% dip)

These results show that the thyristor current comes to an abrupt end when the force commutation signal is applied. These results also show a 4 ms time delay and a 2 ms time delay for the resistive load and the non-linear load respectively.

The force commutation tests for an inductive load were done with a 47 mH inductor and a 14 Ω resistor on the load side (displacement power factor = 0.6). In the case of an inductive load, where the phase voltage and phase current are phase shifted, four states are present where a dip can be initiated. These four states or four quadrants are defined as shown in Figure D.4 a and b, where the flat top waveform (the flat top is caused by the computer power supplies in the Engineering building) represents the supply voltage and the other waveform represents the line current.

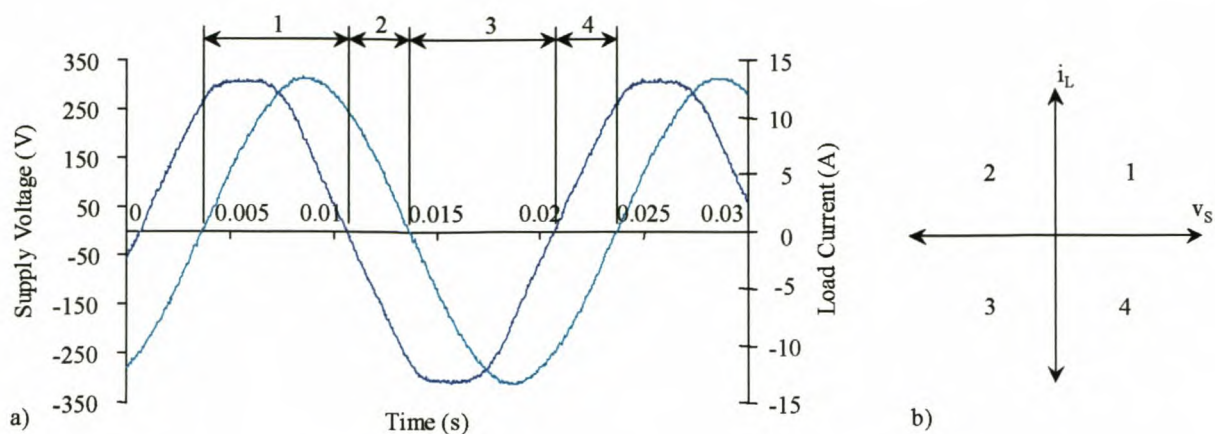


Figure D.4: Four states where force commutation can occur in the case of dip compensation with an inductive load. These states are represented by a) waveforms and b) a two-dimensional vector plane.

The critical states, as explained in the chapter on control, occur where the polarities of the voltage and the current differ. Force commutation is shown in all four of these states in Figure D.5 – Figure D.8. In these results a variac was used to reduce the supply voltage. The reverse recovery current (I_{RRC}) can also be distinguished in Figure D.6 – Figure D.8 in the form of a spike.

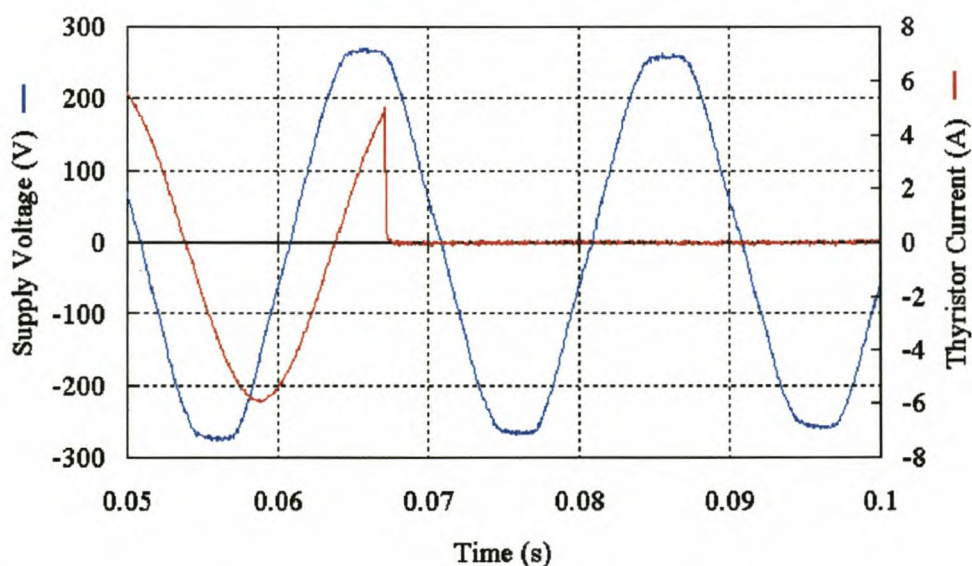


Figure D.5: Force commutation for an inductive load in the first quadrant at the beginning of a 15% dip.

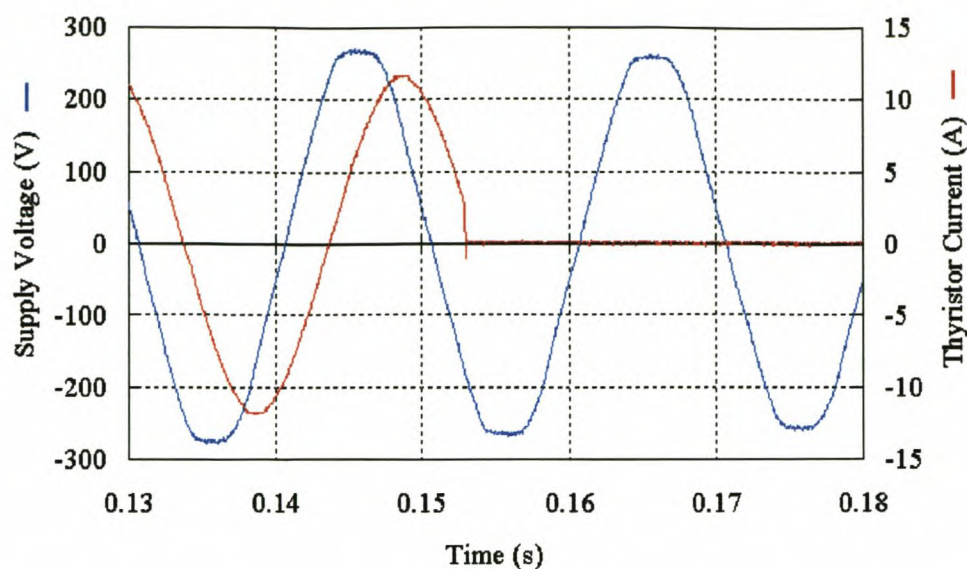


Figure D.6: Force commutation for an inductive load in the second quadrant.

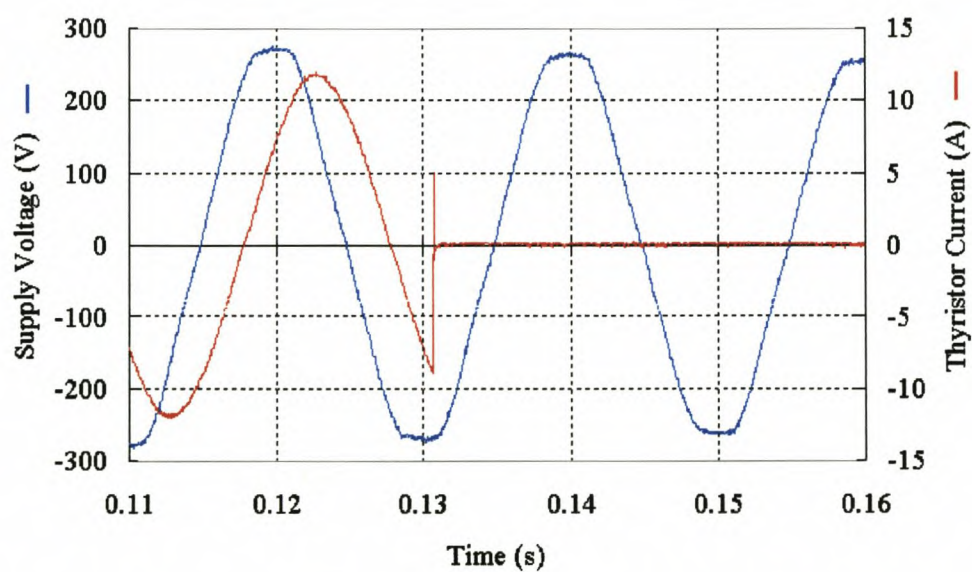


Figure D.7: Force commutation for an inductive load in the third quadrant.

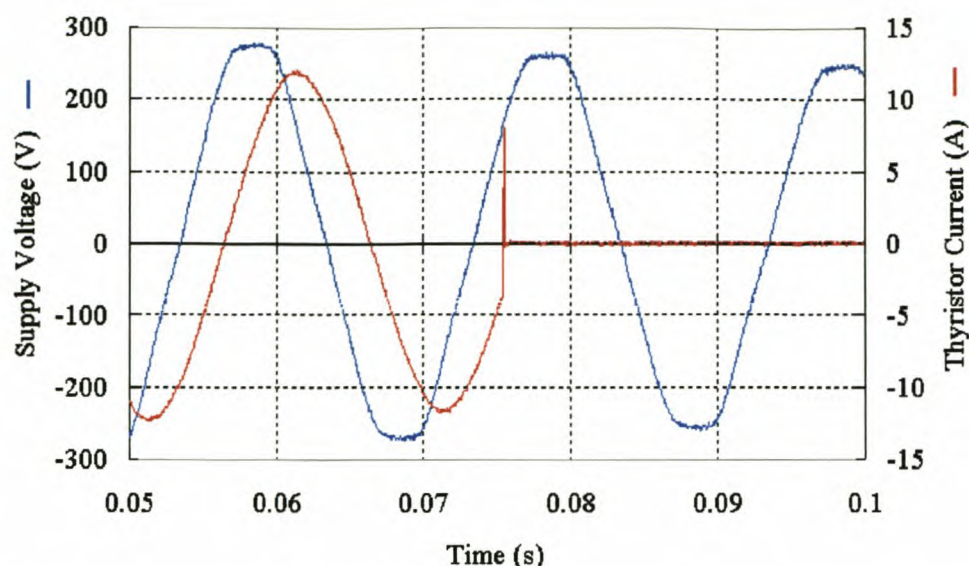


Figure D.8: Force commutation for an inductive load in the fourth quadrant.

c) Sharing of the power delivery and power dissipation

This method, when it was applied on the scale model, was based on the integration of the DC bus currents and a fixed switching pattern.

To verify the sharing of the discharge of the DC buses, four separate DC bus currents were measured simultaneously on a four-channel digital oscilloscope. This was done with a non-linear load at a 15% dip. In this case in each cycle typically only three DC buses would supply current. The discrete values of these four currents were numerically integrated and are shown in Figure D.9.

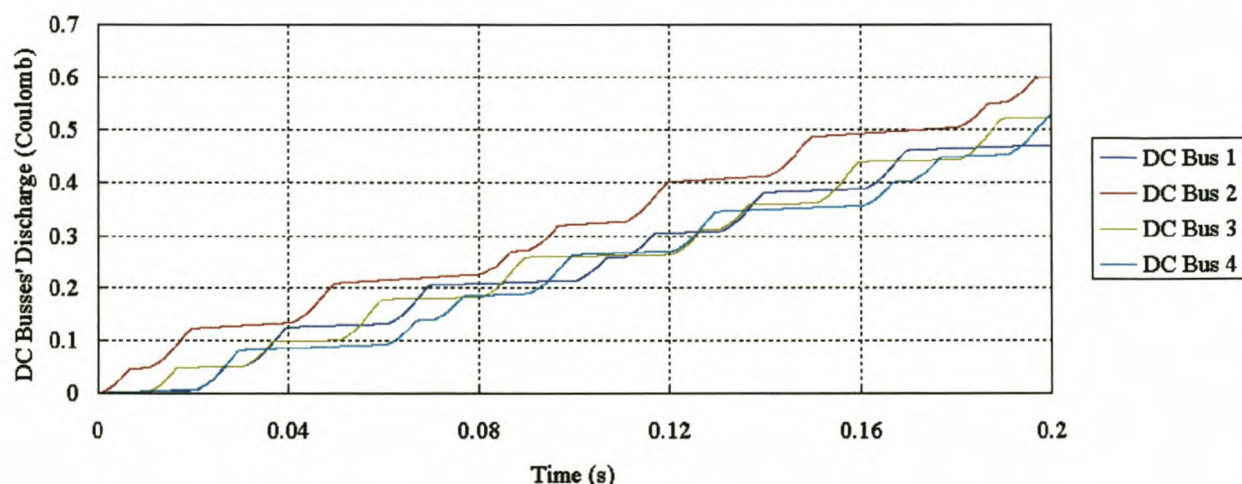


Figure D.9: Discharge of DC buses during dip compensation on a 15% dip with a non-linear load.

This result shows that the discharge of the DC buses over ten cycles in the steady-state part of the dip increase simultaneously. The one discharge curve that deviates slightly from the rest can be attributed to the fact that this current was measured with a different type of current sensor than in the other three cases.

To verify the sharing of the power dissipation in the switching components, the gate signals of four switching components in one inverter were measured. A synchronised measurement of the line current was also taken. The square of the line current was then integrated for the time that each switching component was conducting. Two of these measurements were taken over a period of 500 ms with a non-linear load. Figure D.10 shows this result for a 20% dip and Figure D.11 for a 30% dip. These results showed that the sharing of the power dissipation is more effective for a 30% dip than a lighter dip (20%). These results proved that the method with a fixed switching pattern was not sufficient for the sharing of the power dissipation in the switching components.

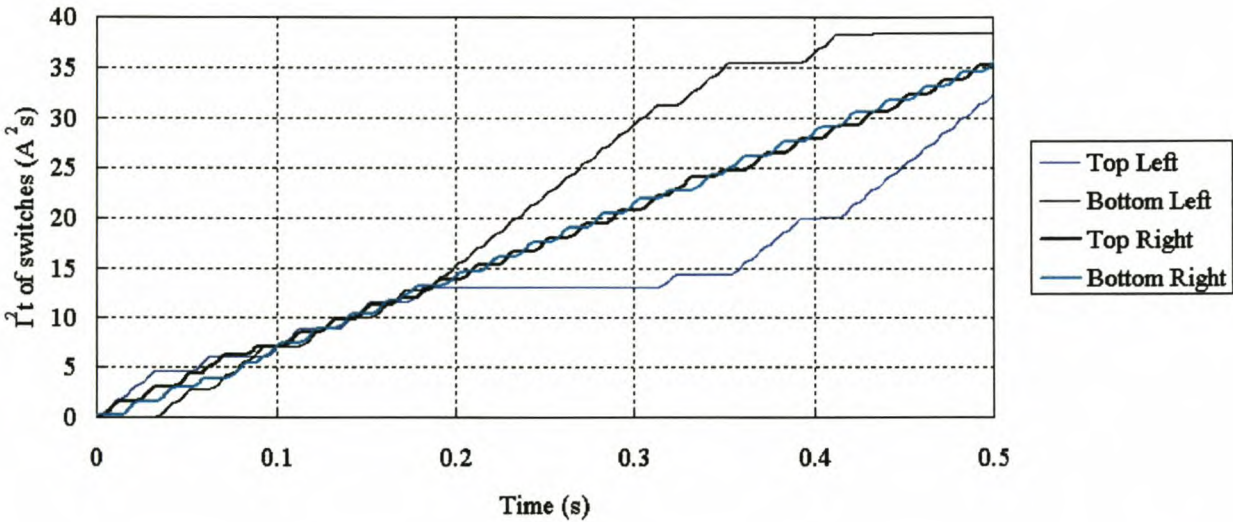


Figure D.10: Estimation of the power dissipation in four switching components of one inverter during a 20% dip with a non-linear load.

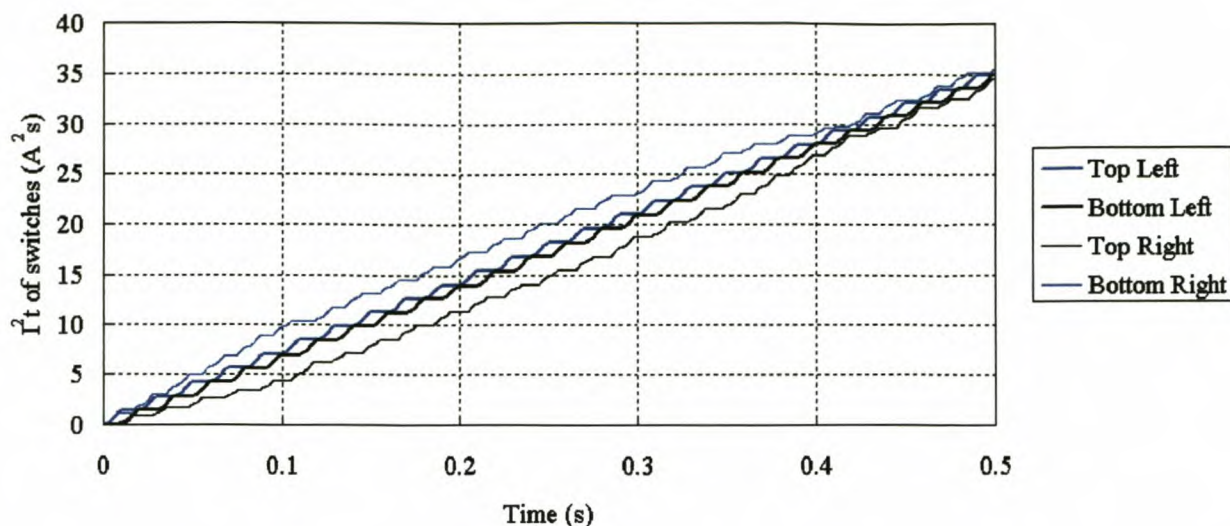


Figure D.11: *Estimation of the power dissipation in four switching components of one inverter during a 30% dip with a non-linear load.*

D.1.2 Dip compensation

In this paragraph the results obtained with the dip generator and a variac are discussed. The dip generator was used to generate two dips at a 220V_{RMS} supply voltage with different depths (15% and 40%), but both with a duration of about 200ms. Another dip at a depth of 30% was manually created with a variac and gives a closer look at the voltage waveforms. These three dips were compensated for three types of loads: resistive, inductive and non-linear. Table D.1 gives a summary of the circumstances present when the results were taken with the dip generator. This table shows the details of the size and the properties of the loads and also the depth of the dips.

The dips with a depth of 40% are more than the specified 30%. These results show that the dip compensator can compensate for deeper dips than specified. The load voltage still complies with NRS048 specifications, in spite of a slight drop, in the case of the 40% depth dips.

A closer look at the voltage waveforms (Figure D.14, Figure D.17, Figure D.20) shows a slight ripple in the load voltages that is caused by the staircase sine waveform. Figure D.20 also shows the non-linearities that are caused by the diode bridge of the non-linear load.

Table D.1: Conditions of the dip compensation results with the scale model and the dip generator/variatic.

| | | | | | | Load characteristics | | |
|--------------|--------|------------------|------------------|------------------|--------------------|-------------------------|-----------------|------------------|
| Type of load | Figure | Depth of dip (%) | Load Current (A) | Load Power (kVA) | Power Factor (DPF) | Resistance (Ω) | Inductance (mH) | Non-linear (y/n) |
| Resistive | D.12 | 15 | 13.5 | 3.04 | 1.0 | 15.9 | — | n |
| | D.13 | 40 | 13.5 | 3.04 | 1.0 | 15.9 | — | n |
| | D.14 | 30 | 11.0 | 2.48 | 1.0 | 19.2 | — | n |
| Inductive | D.15 | 15 | 7.0 | 1.58 | 0.6 | 14.0 | 47.0 | n |
| | D.16 | 40 | 7.0 | 1.58 | 0.6 | 14.0 | 47.0 | n |
| | D.17 | 30 | 7.0 | 1.58 | 0.6 | 14.0 | 47.0 | n |
| Non-linear | D.18 | 15 | 13.0 | 2.93 | 1.0 | 19.5 | 47.0 | y |
| | D.19 | 40 | 13.0 | 2.93 | 1.0 | 19.5 | 47.0 | y |
| | D.20 | 30 | 13.0 | 2.93 | 1.0 | 19.5 | 47.0 | y |

a) Dip compensation with a resistive load

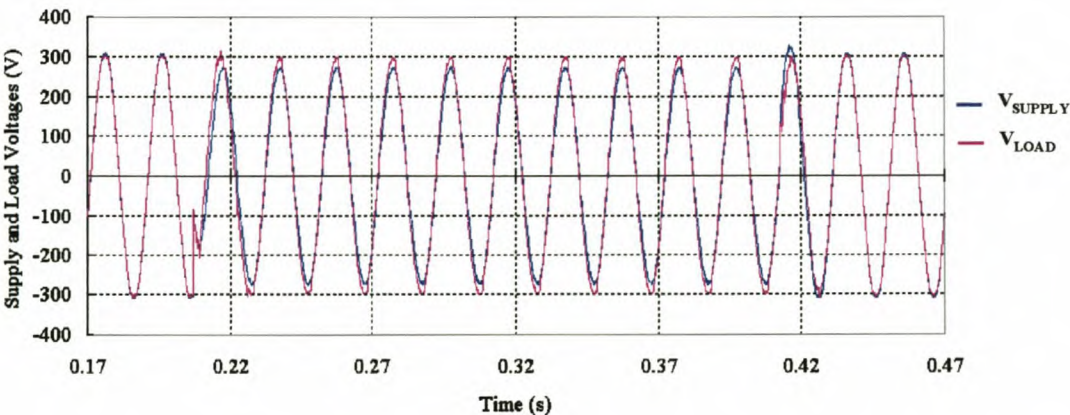


Figure D.12: Dip compensation on a resistive load with a dip depth of 15%.

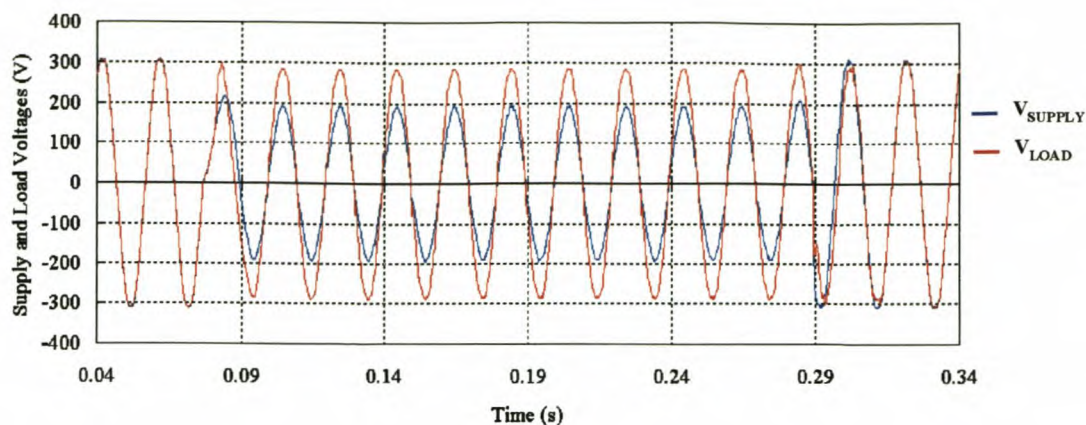


Figure D.13: *Dip compensation on a resistive load with a dip depth of 40%.*

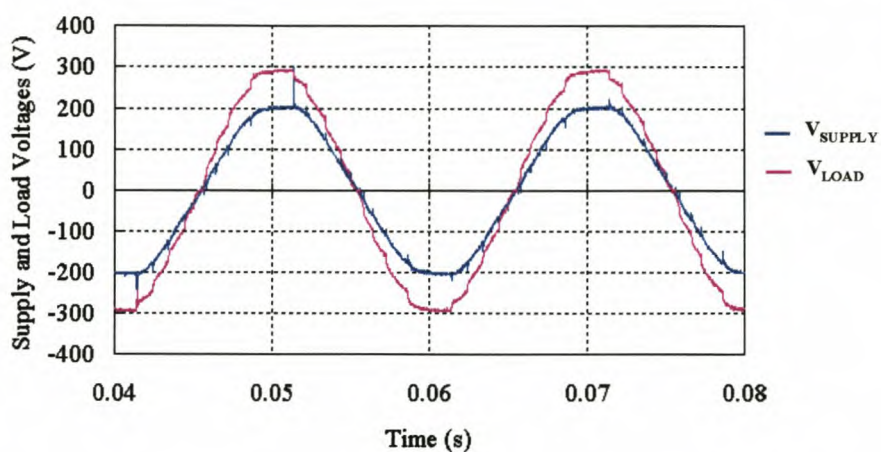


Figure D.14: *Dip compensation on a resistive load with a dip depth of 30%.*

b) Dip compensation with an inductive load

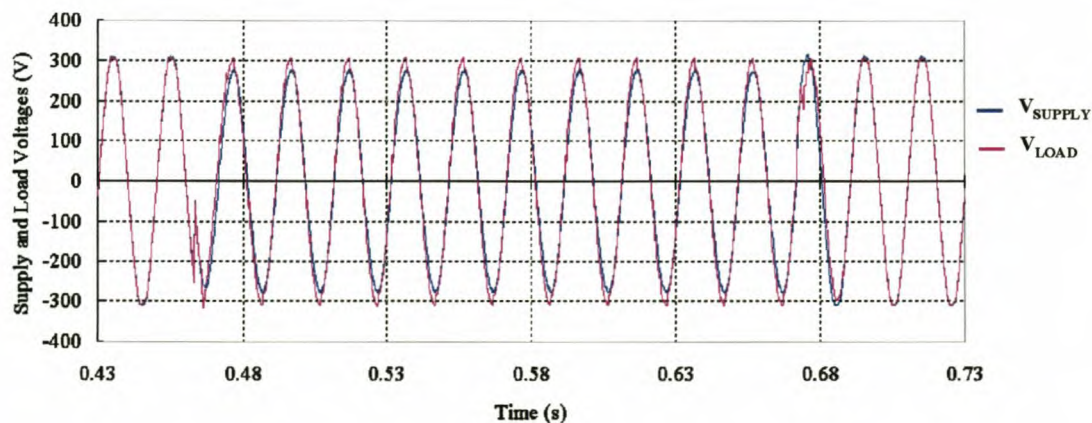


Figure D.15: *Dip compensation on an inductive load with a dip depth of 15%.*

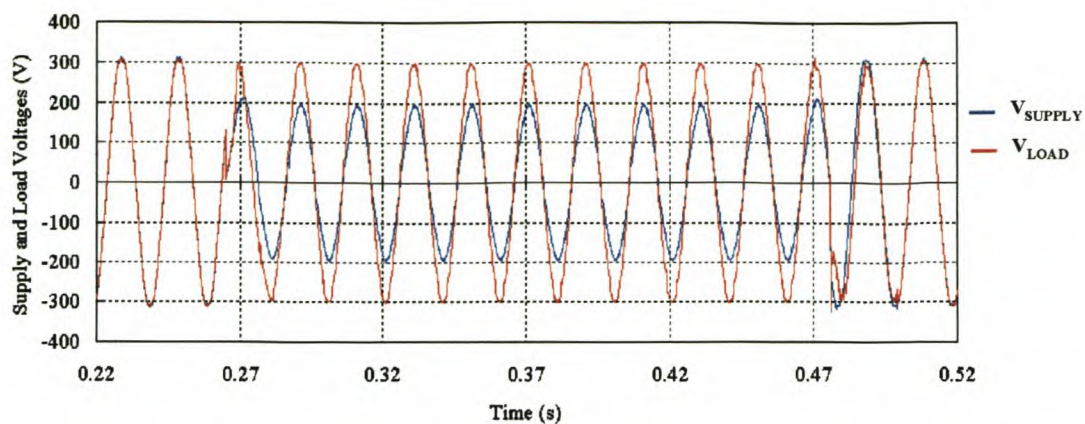


Figure D.16: *Dip compensation on an inductive load with a dip depth of 40%.*

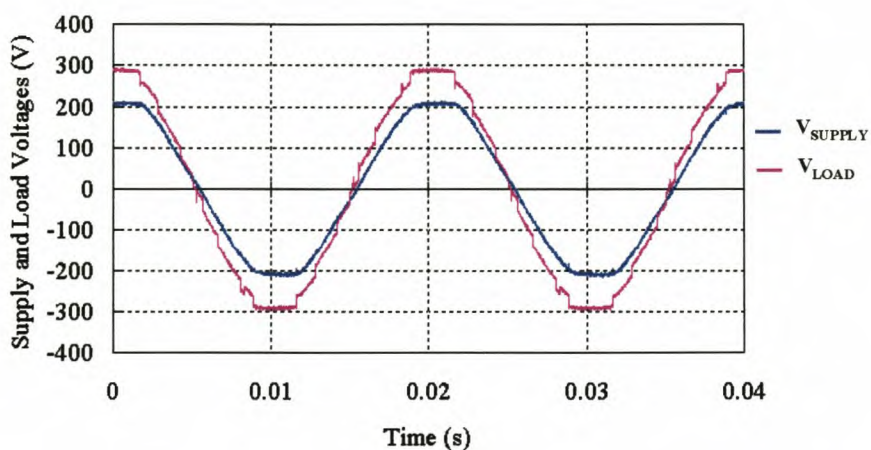


Figure D.17: *Dip compensation on an inductive load with a dip depth of 30%.*

c) Dip compensation with a non-linear load

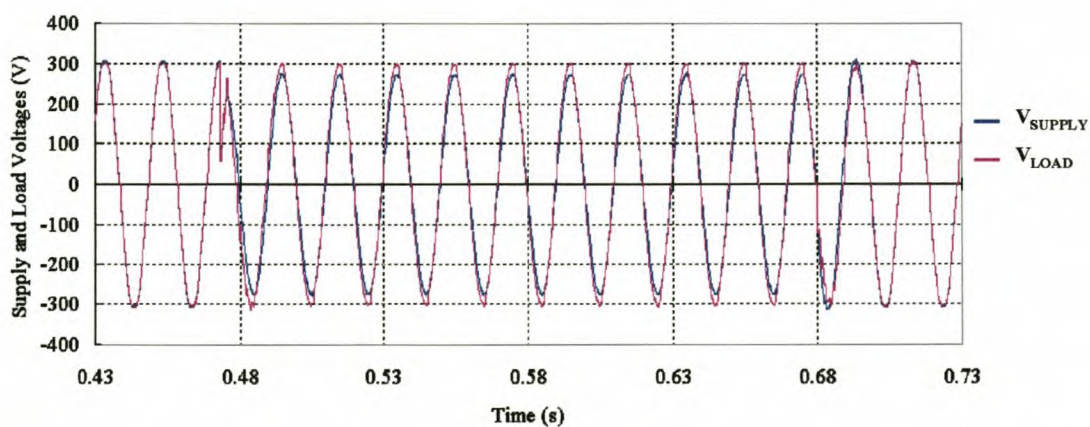


Figure D.18: *Dip compensation on a non-linear load with a dip depth of 15%.*

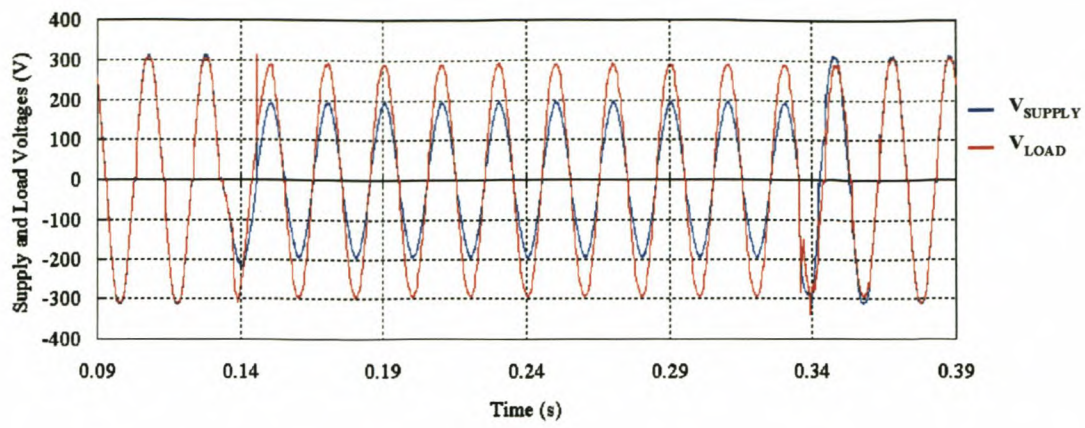


Figure D.19: *Dip compensation on a non-linear load with a dip depth of 40%.*

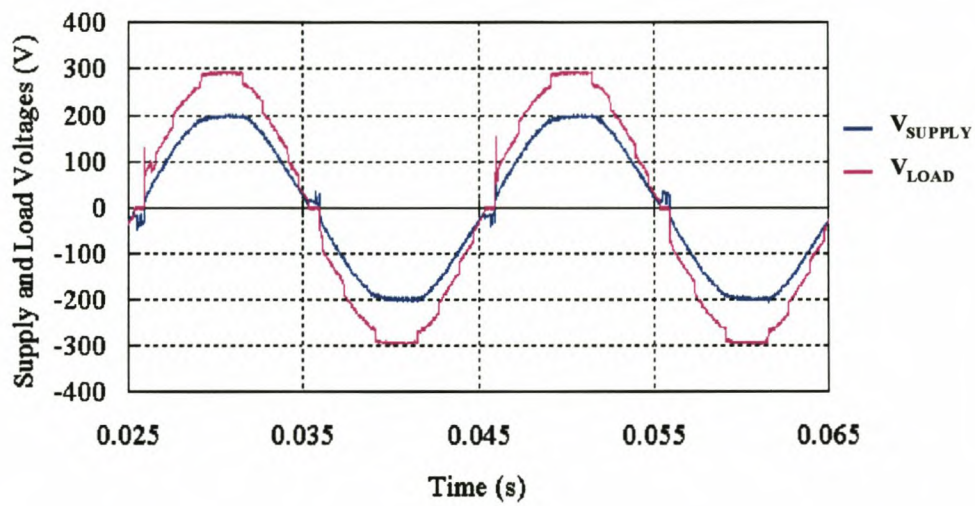


Figure D.20: *Dip compensation on a non-linear load with a dip depth of 30%.*

D.2 Other tests on single inverter

These tests were conducted in the same way as the ones described in paragraph 6.2.

D.2.1 Staircase load current with a 220 A amplitude

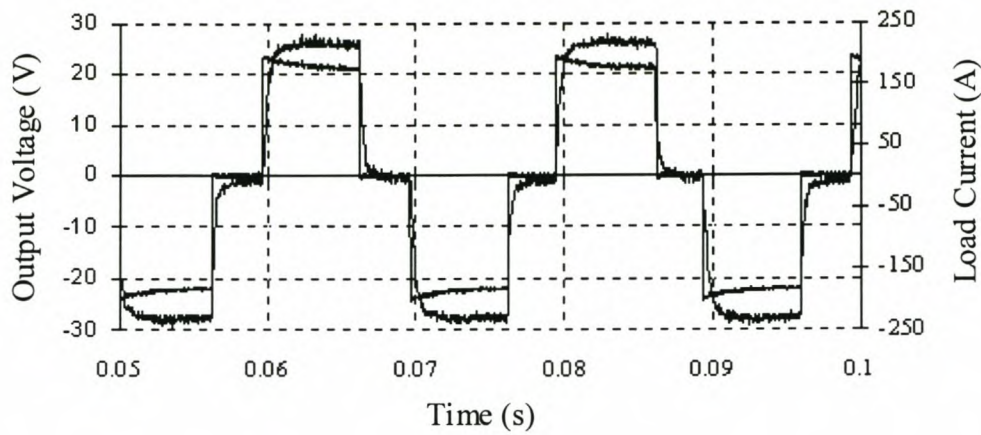


Figure D.21: Square wave load voltage and current (220 A amplitude) for a single inverter.

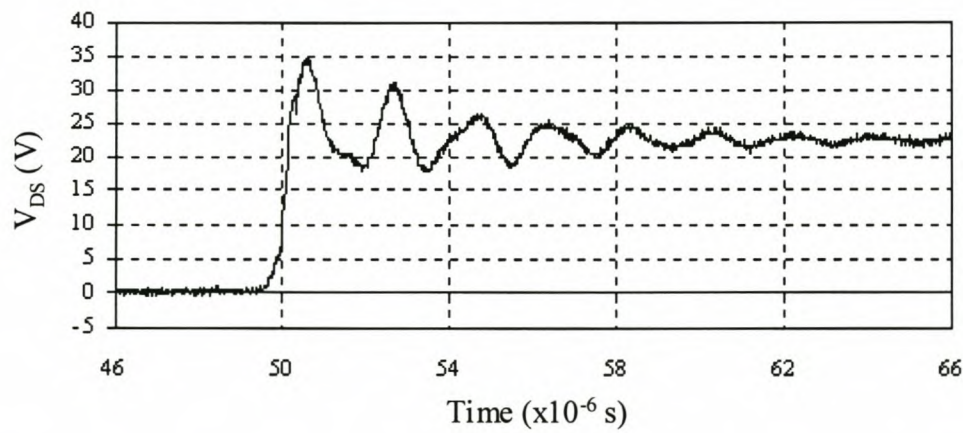


Figure D.22: Drain-source voltage of the MOSFETs at turn-off for a load current of 220 A.

D.2.2 Staircase load current with a 300 A amplitude

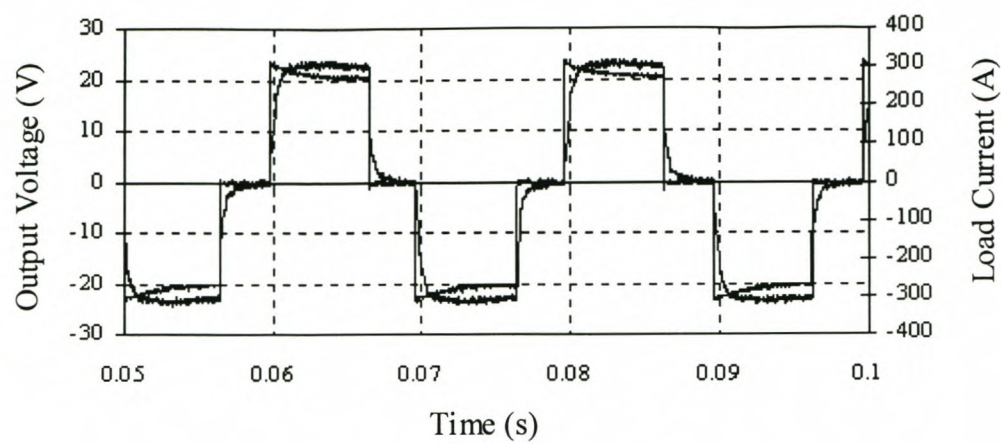


Figure D.23: Square wave load voltage and current (300 A amplitude) for a single inverter.

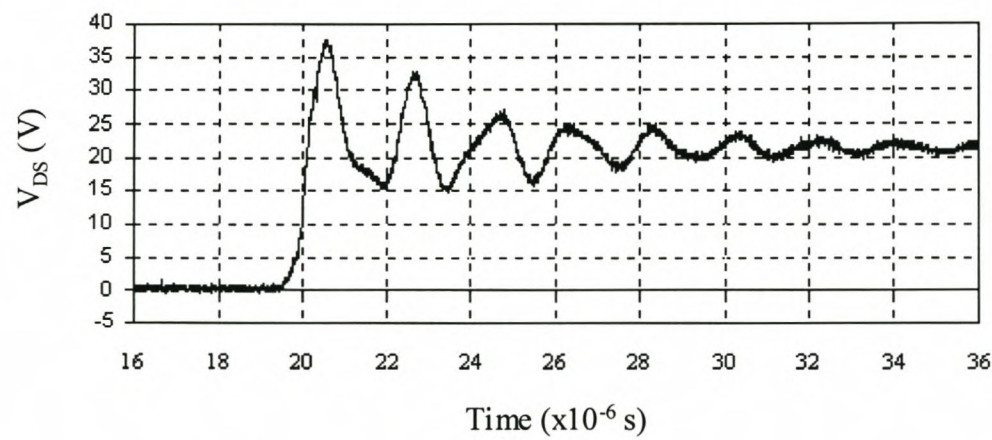


Figure D.24: Drain-source voltage of the MOSFETs at turn-off for a load current of 300 A.

D.2.3 Staircase load current with a 420 A amplitude

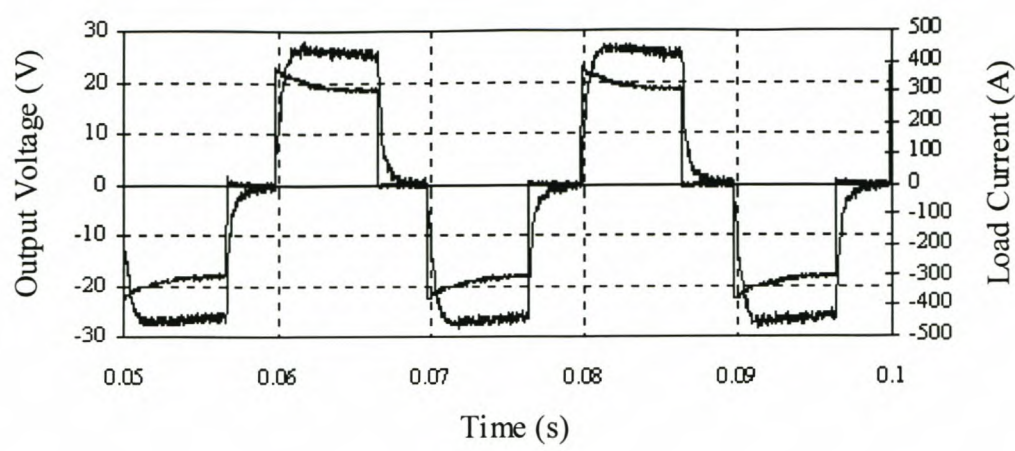


Figure D.25: Square wave load voltage and current (420 A amplitude) for a single inverter.

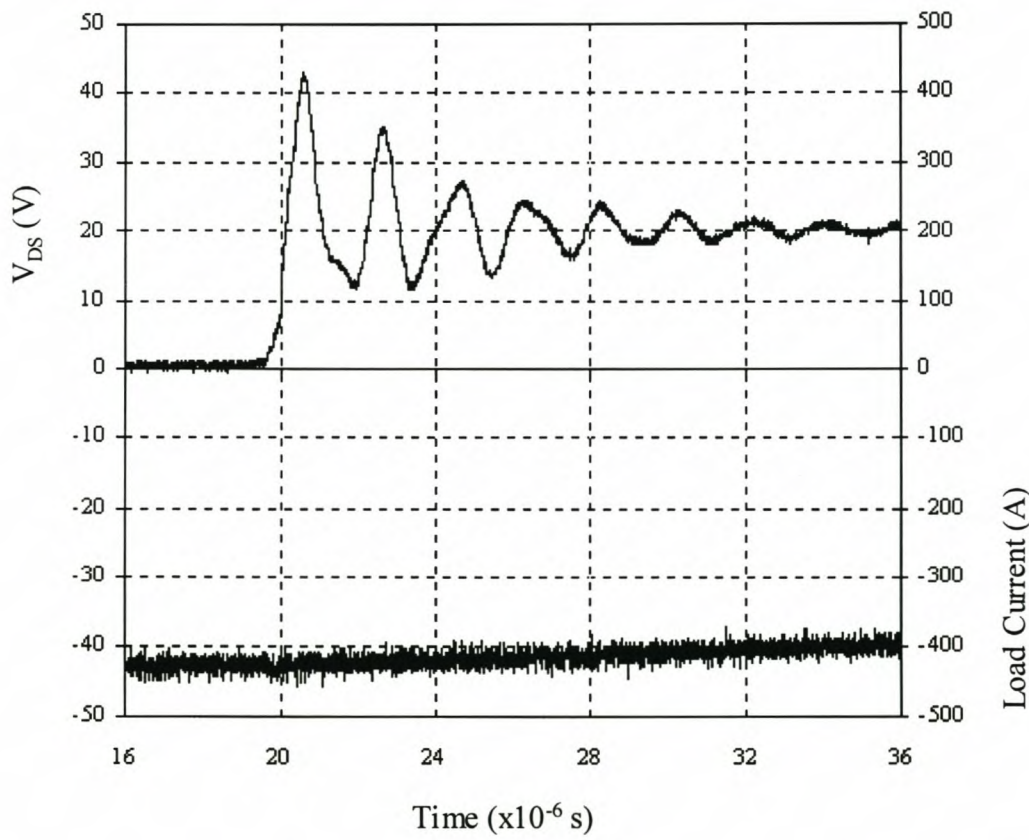


Figure D.26: Drain-source voltage of the MOSFETs at turn-off for a load current of 420 A.

D.2.4 Staircase load current with a 480 A amplitude

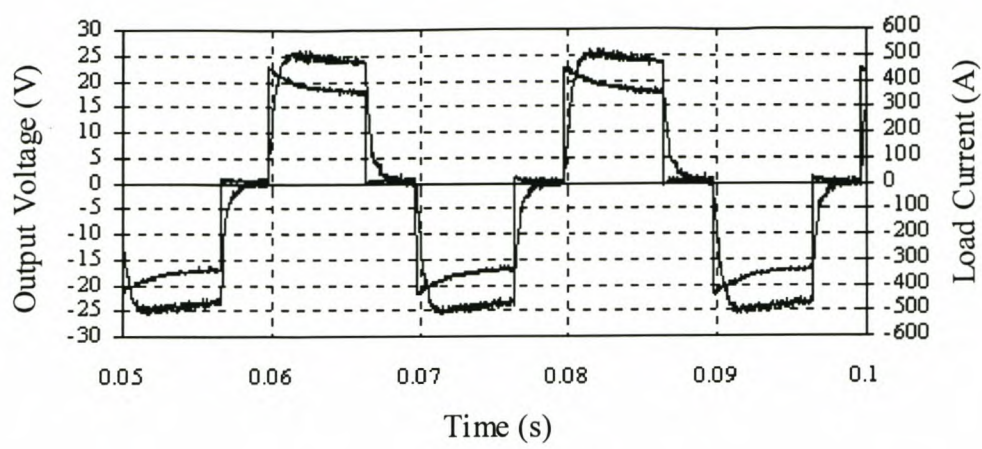


Figure D.27: Square wave load voltage and current (480 A amplitude) for a single inverter.

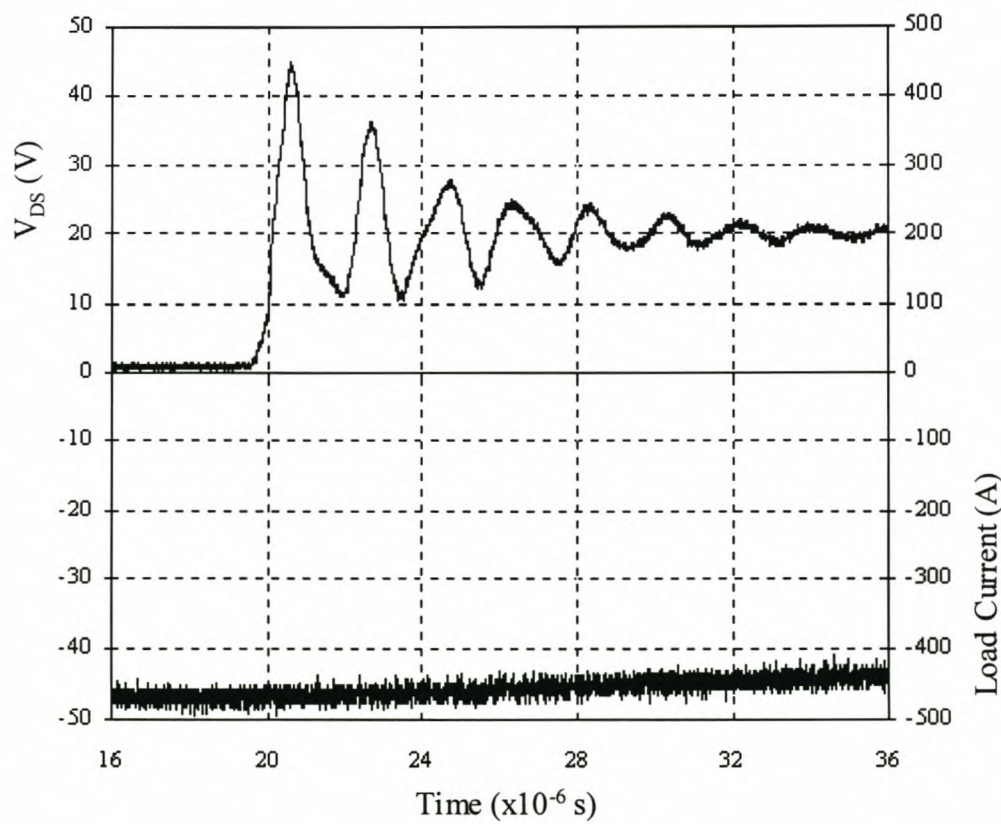


Figure D.28: Drain-source voltage of the MOSFETs at turn-off for a load current of 480 A.

D.3 Other tests on the full-scale dip compensator

This part of the Appendix contains similar results to the ones presented in Chapter 6. Three other results on the drain-source voltage of the MOSFETs at turn-off are shown in Figure D.29 – Figure D.31. Also note here that the battery voltage plays a role in the value of V_{DSmax} . This voltage will depend on how much the batteries have been discharged at that stage and also on the switching state before turn-off, i.e. if the inverter was in the zero state (states 1 and 3 of Figure 5.14) or not.

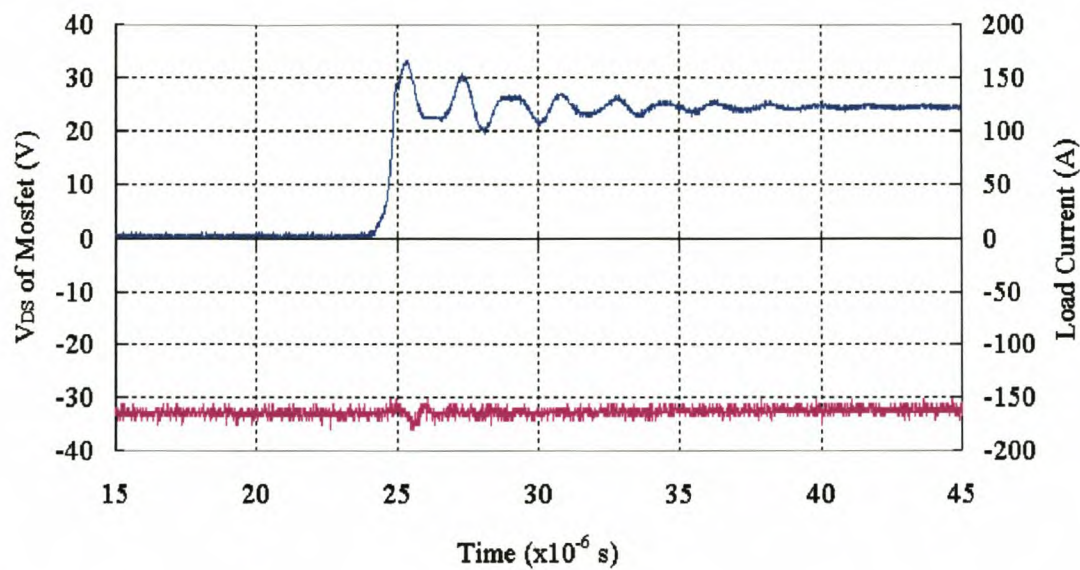


Figure D.29: Drain-source voltage of the MOSFETs at turn-off for a load current of 164 A.

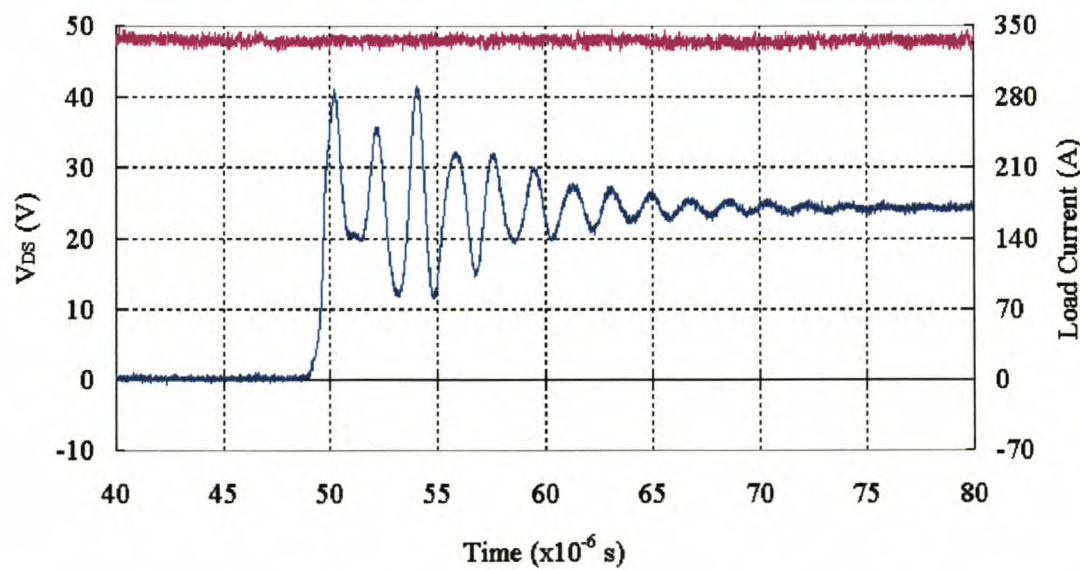


Figure D.30: Drain-source voltage of the MOSFETs at turn-off for a load current of 336 A.

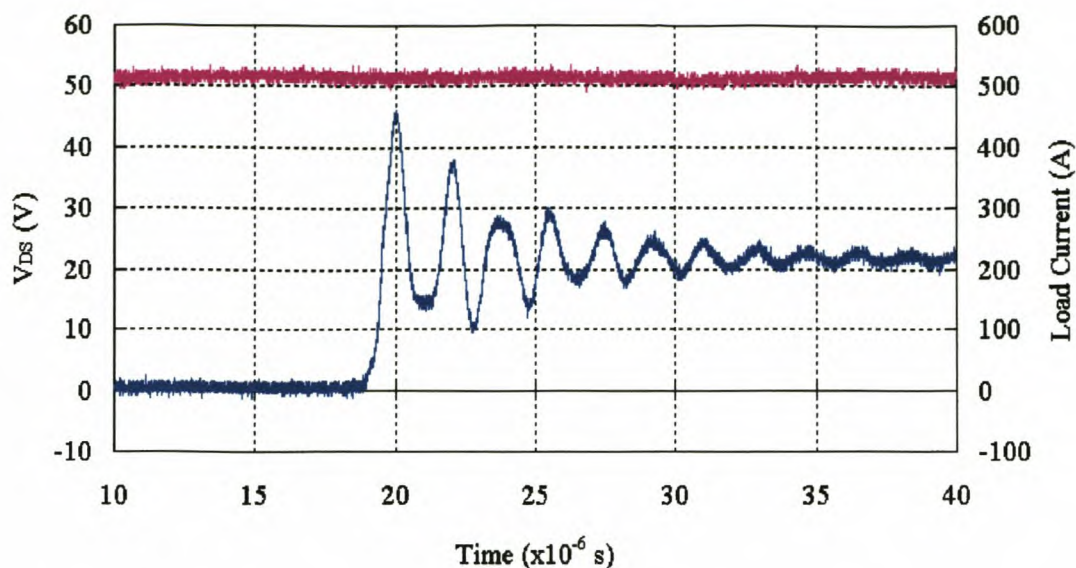


Figure D.31: Drain-source voltage of the MOSFETs at turn-off for a load current of 515 A.

Figure D.32 shows force commutation of the thyristor for a 208 A_{RMS} non-linear load current taken for a 31% dip depth.

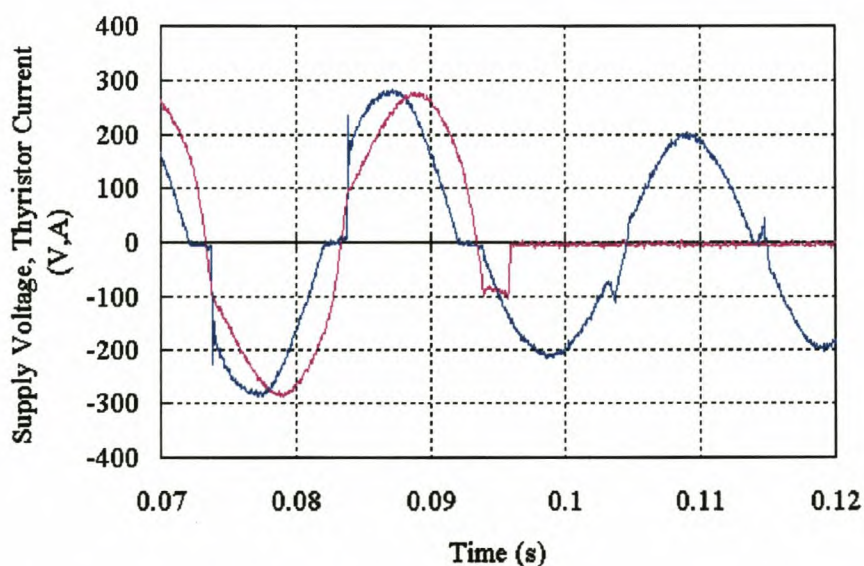


Figure D.32: Force commutation for a 31% dip at a 208 A_{RMS} non-linear load current.

The rest of this paragraph shows dip compensation results for the same basic conditions stated at the beginning of paragraph 6.3. Table D.2 summarises the other specific conditions for these results.

Table D.2: Specific conditions of the dip compensation results with the full-scale dip compensator.

| | | | | | | Load characteristics | |
|--------------|--------|------------------|-------------------------|------------------|--------------------|-------------------------|-----------------|
| Type of load | Figure | Depth of dip (%) | Value of L_{DIP} (mH) | Load Current (A) | Power Factor (DPF) | Resistance (Ω) | Inductance (mH) |
| Resistive | D.33 | 28 | 0.8 | 73 | 1.0 | 3.6 | — |
| | D.34 | 32 | 0.8 | 134 | 1.0 | 1.8 | — |
| | D.35 | 35 | 0.8 | 220 | 1.0 | 1 | — |
| Inductive | D.36 | 43 | 1.2 | 150 | 0.75 | 0.9 | 1.8 |
| | D.37 | 28 | 0.8 | 160 | 0.79 | 0.9 | 1.8 |
| Non-linear | D.38 | 46 | 1.2 | 140 | 1.0 | 1.4 | 1.8 |
| | D.39 | 30 | 0.8 | 150 | 1.0 | 1.4 | 1.8 |
| | D.40 | 47 | 1.2 | 156 | 1.0 | 1.2 | 1.8 |
| | D.41 | 31 | 0.8 | 166 | 1.0 | 1.2 | 1.8 |
| | D.42 | 31 | 0.8 | 208 | 1.0 | 0.9 | 1.8 |
| | D.43 | 37 | 0.8 | 318 | 1.0 | 0.4 | 1.8 |

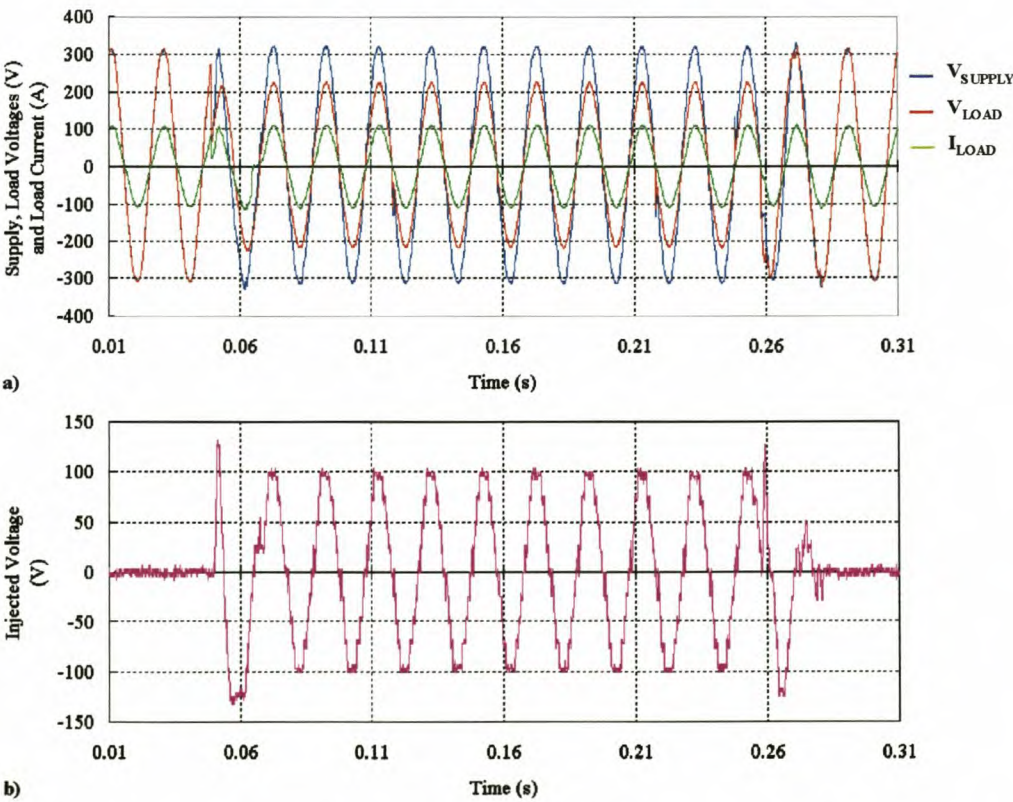


Figure D.33: Dip compensation on a 28% dip for a resistive load at 73 A_{RMS} .

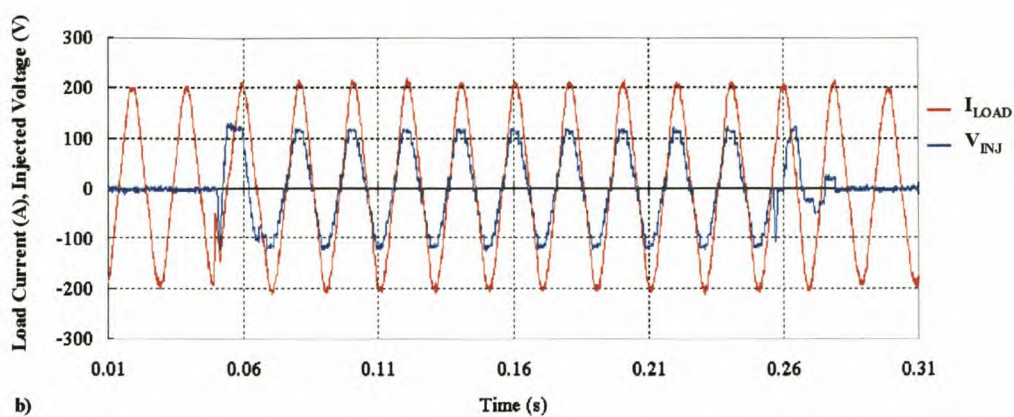
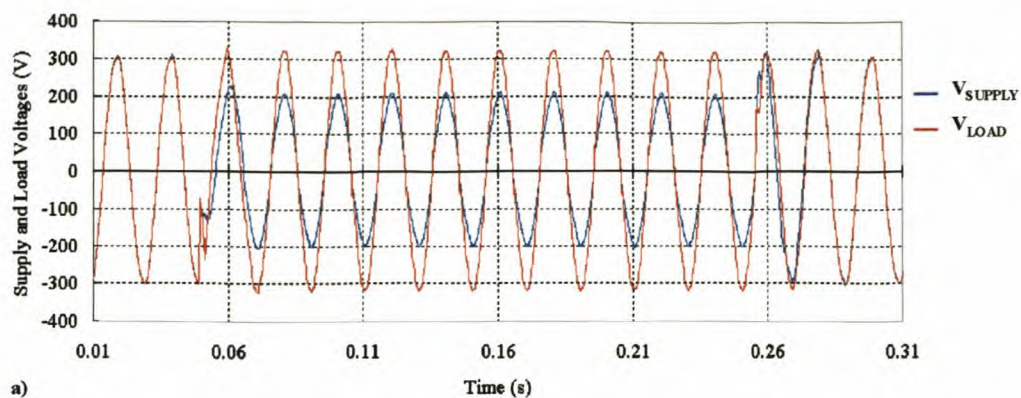


Figure D.34: Dip compensation on a 32% dip for a resistive load at $134 A_{RMS}$.

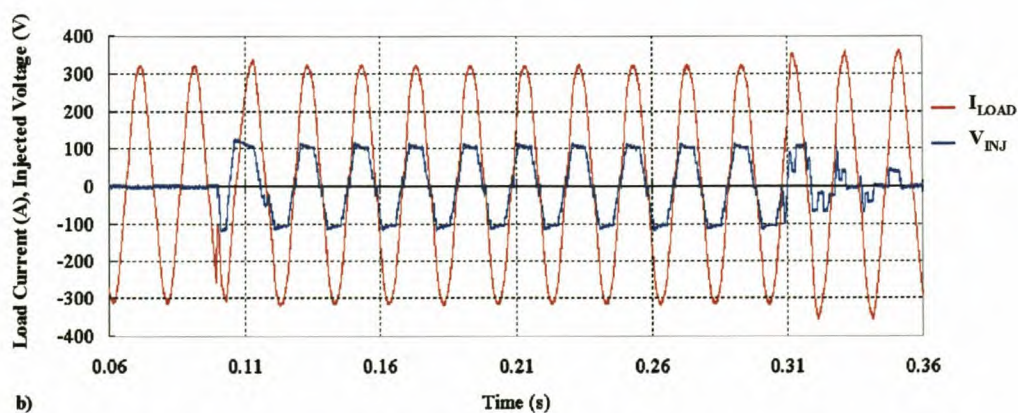
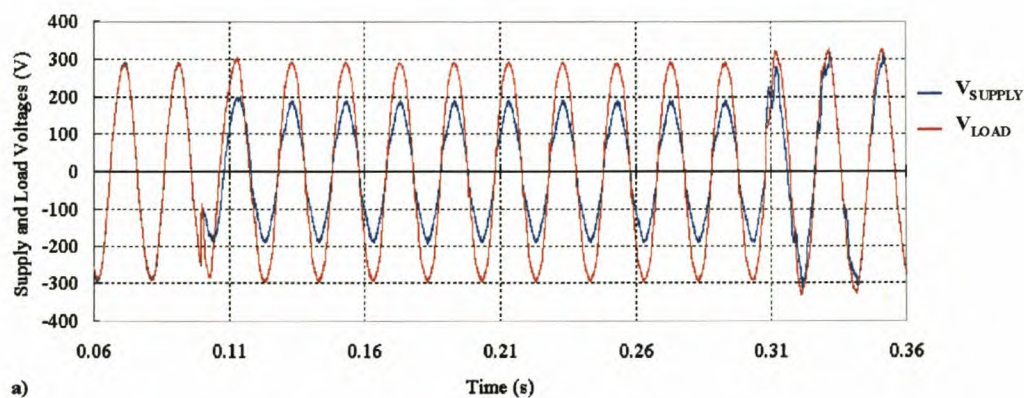


Figure D.35: Dip compensation on a 35% dip for a resistive load at $220 A_{RMS}$.

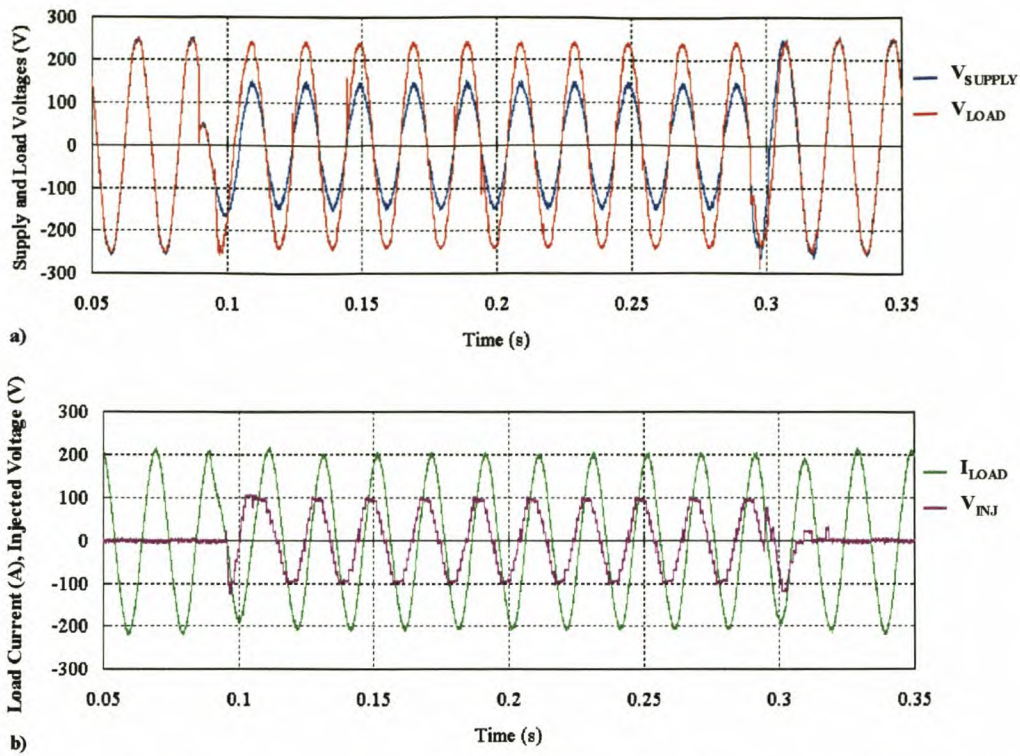


Figure D.36: Dip compensation on a 43% dip for an inductive load at $150 A_{\text{RMS}}$.

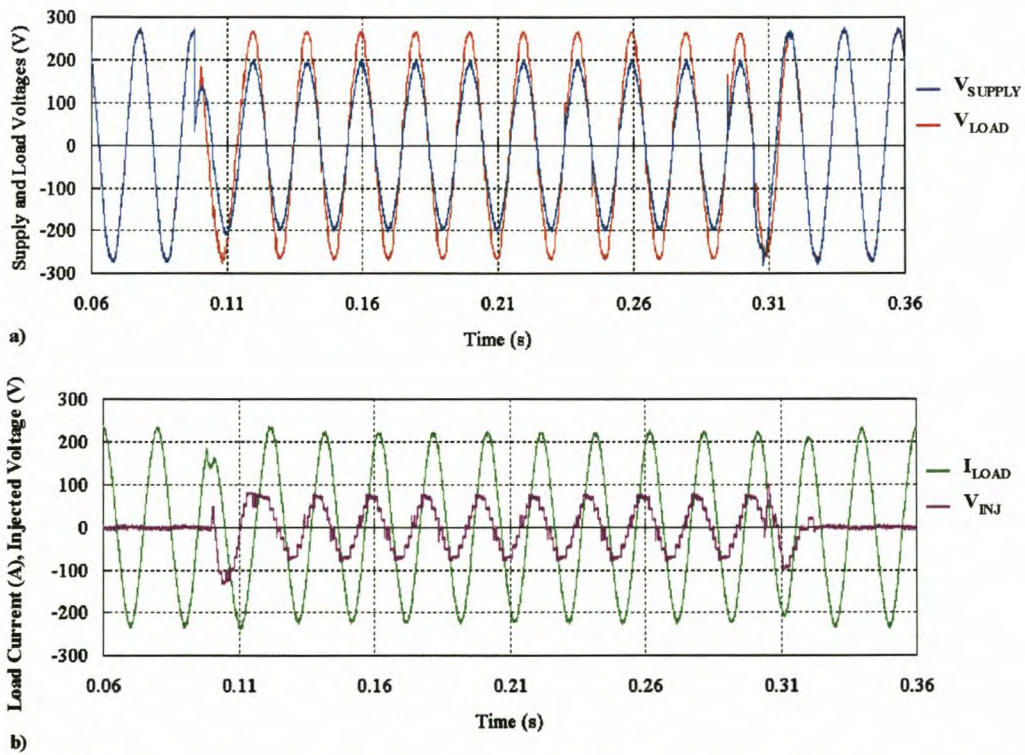


Figure D.37: Dip compensation on a 28% dip for an inductive load at $160 A_{\text{RMS}}$.

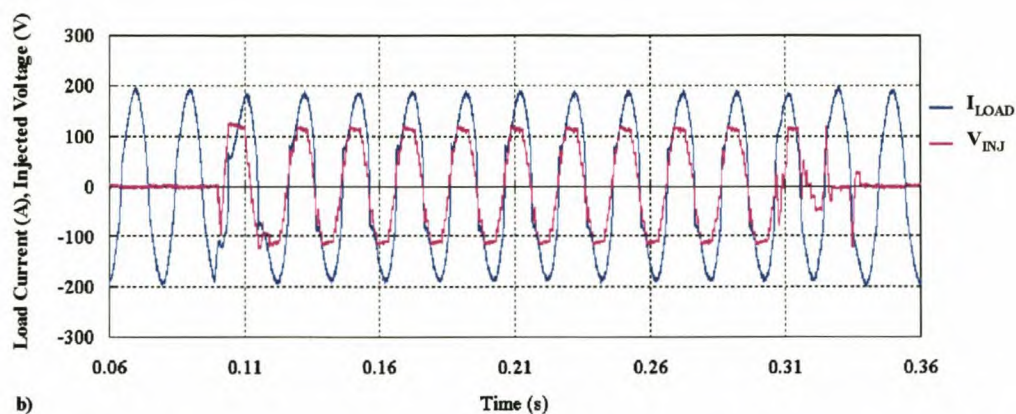
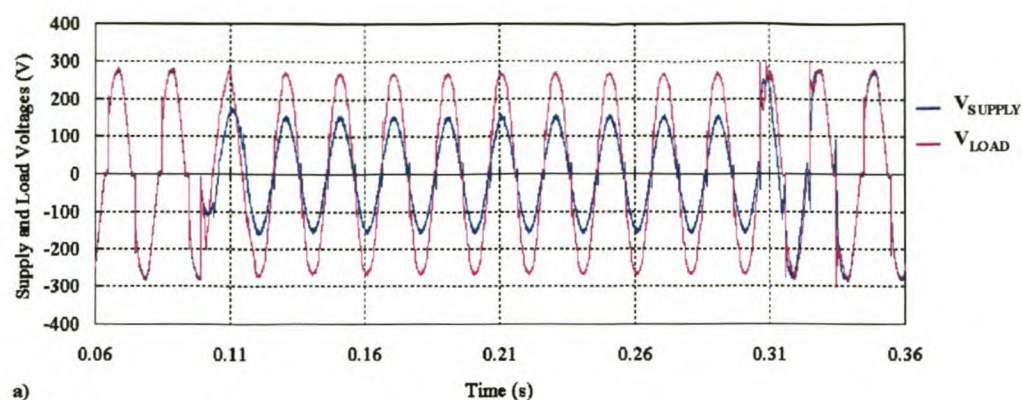


Figure D.38: Dip compensation on a 46% dip for a non-linear load at $140 A_{\text{RMS}}$.

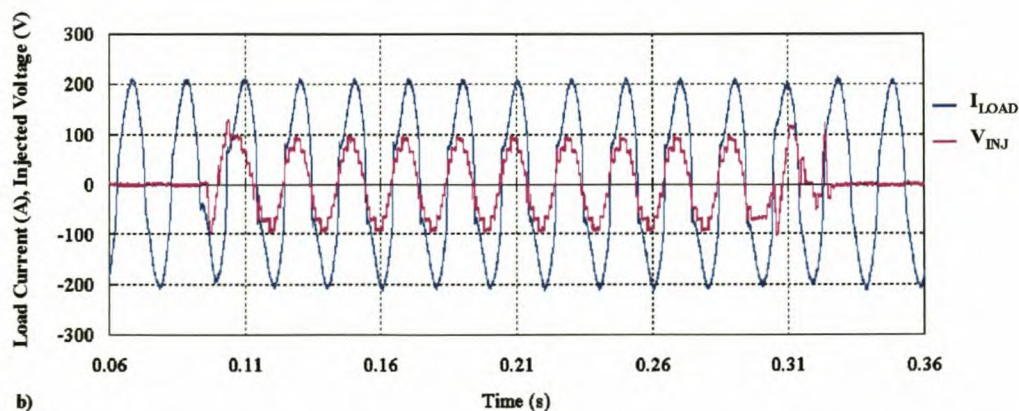
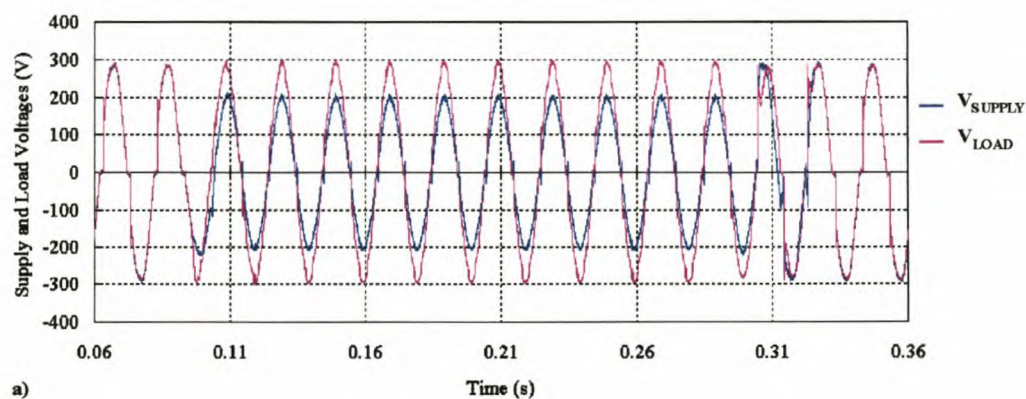


Figure D.39: Dip compensation on a 30% dip for a non-linear load at $150 A_{\text{RMS}}$.

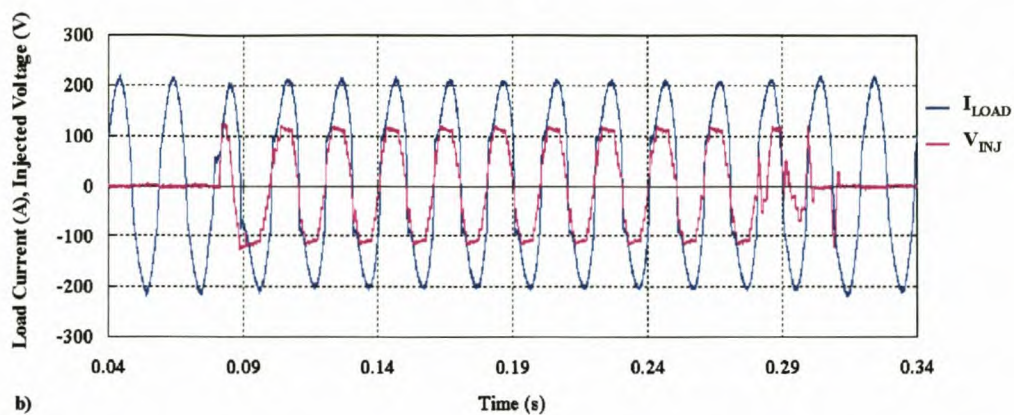
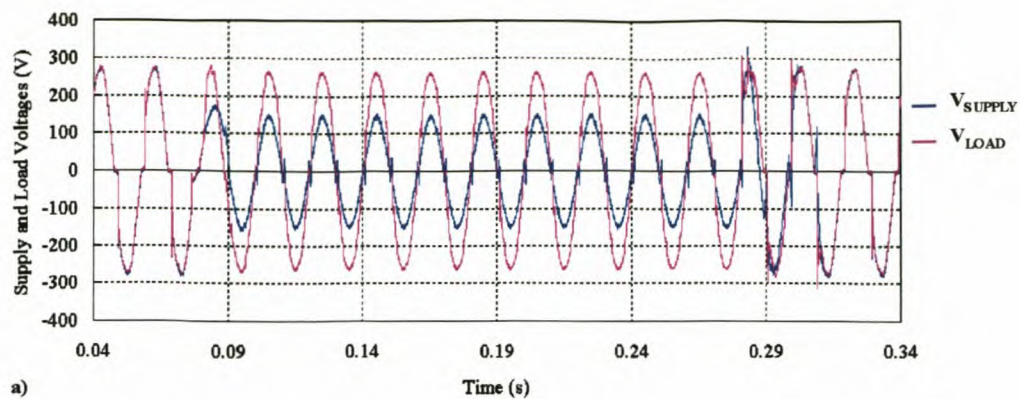


Figure D.40: Dip compensation on a 47% dip for a non-linear load at $156 A_{RMS}$.

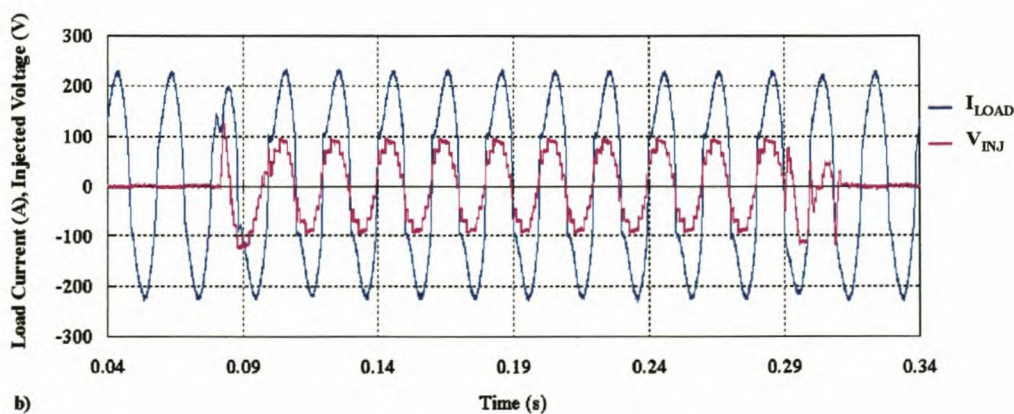
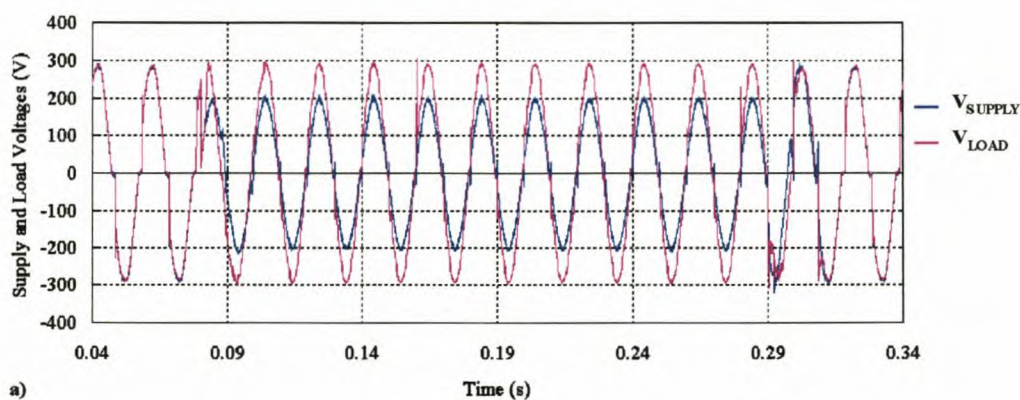


Figure D.41: Dip compensation on a 31% dip for a non-linear load at $166 A_{RMS}$.

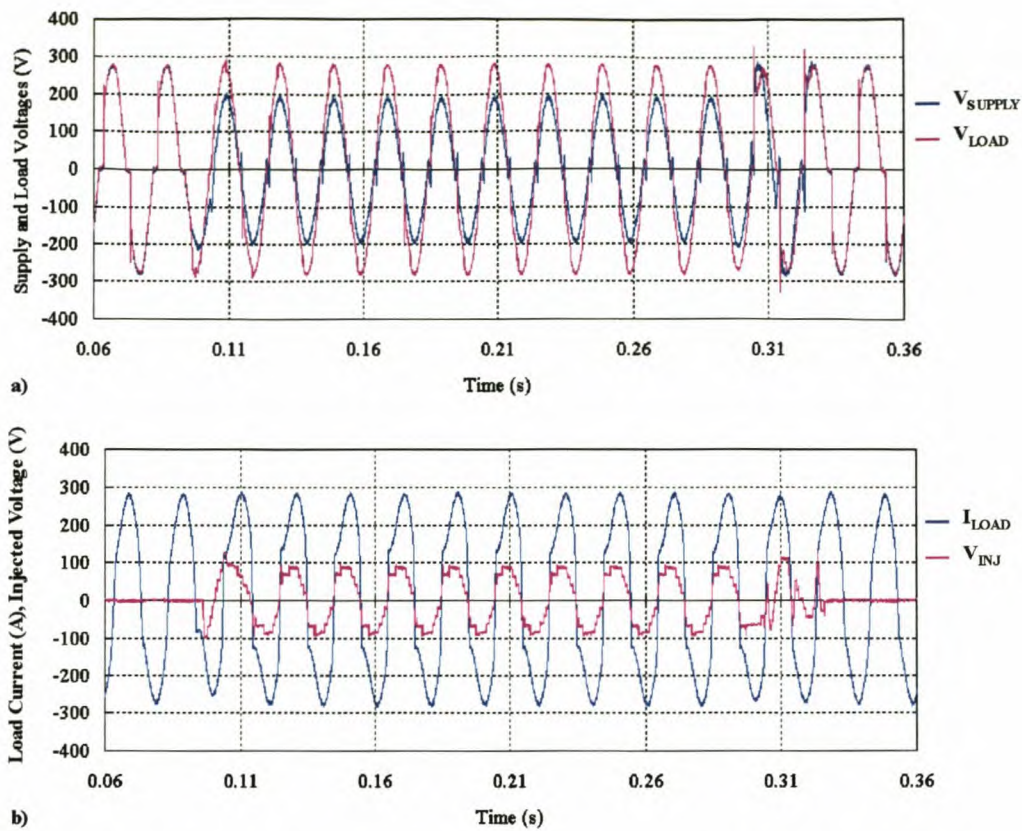


Figure D.42: Dip compensation on a 31% dip for a non-linear load at 208 A_{RMS} .

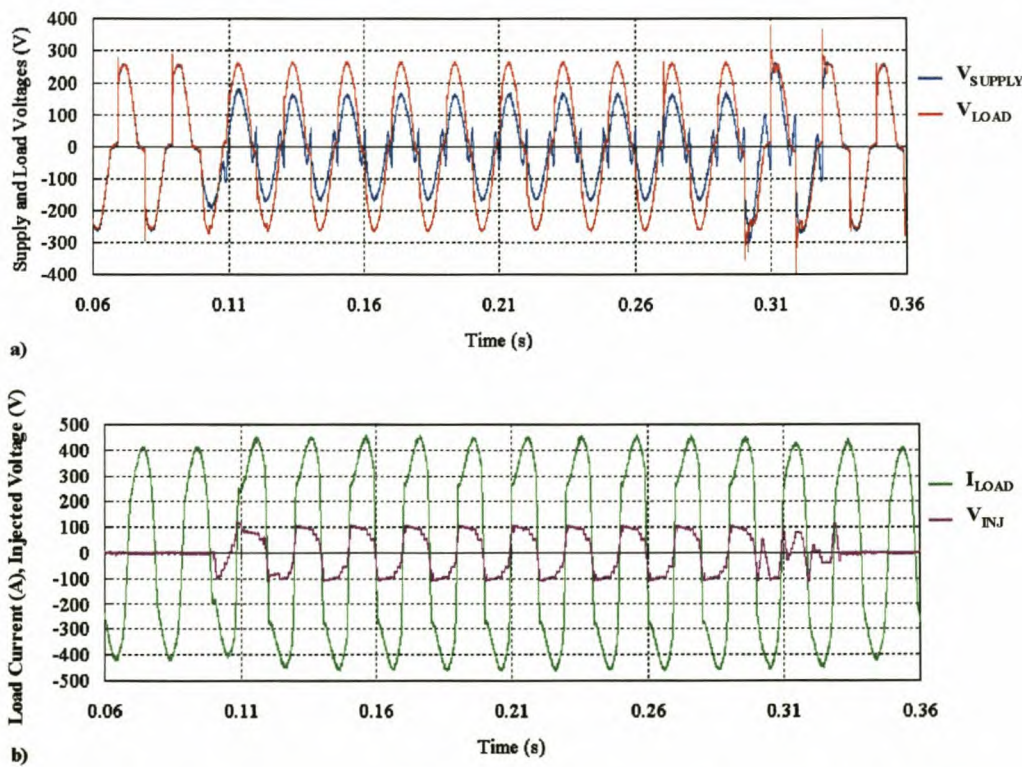


Figure D.43: Dip compensation on a 37% dip for a non-linear load at 318 A_{RMS} .